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Non-volatile magnetic random access memories (MRAM)

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Abstract

Magnetic random access memories (MRAM) are a new non-volatile memory technology trying establish itself as a mainstream technology. This paper reviews briefly the most important progress realized in the past 10 years. Basic MRAM cell operation is described as well as the main subsisting design challenges. Special emphasis is placed on bit write strategies and their respective scaling perspectives. ***To cite this article: R.C. Sousa, I.L. Prejbeanu, C. R. Physique 6 (2005).***
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Résumé

Mémoires magnétiques non-volatiles à access aleatoire. Les mémoires magnétiques à access aléatoire (MRAM) sont une nouvelle technologie de mémoires non volatiles cherchant à s'imposer comme une technologie majeure. Cet article fait un resumé des progrès les plus importants realisés au cours des 10 dernières années. Le mode de fonctionnement des MRAM est décrit ainsi que les défis qui subsistent encore pour leur réalisation. Les diverses stratégies d'écriture et leurs perspectives en termes de réduction de taille de cellule sont discutées. ***Pour citer cet article : R.C. Sousa, I.L. Prejbeanu, C. R. Physique 6 (2005).***
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Mots-clés : MRAM ; Jonctions tunnel magnétiques ; Mémoire

1. Introduction

Magnetism contributes greatly to the goal of storing information for long time periods (10 years), in the form of hard disk drive and magnetic tape storage systems. In these two examples data, access time is limited by the fact that these are mechanical systems. Only solid state memories like Dynamic Random Access Memory (DRAM) and the Static Random Access Memory (SRAM) are capable of ns access times in both read and write operations. These memories are volatile and data is stored only as long as power is supplied to refresh the capacitor charge in DRAM and to keep the transistors on in SRAM. The need for a non-volatile memory is reflected in the increasing demand for Flash memory, fueled by its use in digital consumer products. However Flash technology suffers from slow write access time in the μs range and poor bit cyclability limited to 10^6 write events. Magnetic random access memories (MRAM) is one technology proposing to close the performance gap between existing volatile and non-volatile memory technologies. Other alternatives are ferroelectric random access memories (FeRAM) based on ferroelectric materials and phase change based Ovonyx unified memory (OUM). The most important characteristics of all these

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Table 1
Comparison of memory technologies

Feature	DRAM	SRAM (6T)	FLASH	OUM	MRAM	FeRAM
Cell size [F^2]	8–12	50–80	4–11	5–8	6–20	4–16
Non-volatile	No	No	Yes	Yes	Yes	Yes
Endurance write/read	∞/∞	∞/∞	$10^6/\infty$	$>10^{12}/\infty$	$>10^{15}/\infty$	$>10^{12}/>10^{12}$
Non-destructive read	No	Partial	Yes	Yes	Yes	No
Direct overwrite	Yes	Yes	No	Yes	Yes	Yes
Signal margin	100–200 mV	100–200 mV	Δ current	10–100 × R	60–200% R	100–200 mV
Write/read	50 ns/50 ns	8 ns/8 ns	200 μs/60 ns	10 ns/20 ns	30 ns/30 ns	80 ns/80 ns
Erase	50 ns	8 ns	1–100 ms (block)	50 ns	30 ns	80 ns
Transistor performance	Low	High	High voltage (HV)	High	High	High
Scalability limits	Capacitor	6 Transistors	Tunnel oxide/HV	Litho.	Current density	Capacitor

memory types are summarized in Table 1. MRAM devices have already been demonstrated based on giant magnetoresitive (GMR) elements [1] and more recently using magnetic tunnel junctions (MTJ) [2,3]. This paper reviews the principles in MTJ based MRAMs and highlights the latest developments and new approaches being investigated.

2. Conventional MRAM operation

The basic MRAM cell element consists of a magnetic tunnel junction structure in which two ferromagnetic electrodes are separated by a thin insulating barrier. The tunneling current flowing through the structure depends upon the relative orientation of the magnetization in both electrodes. The resistance change between the low resistance parallel alignment and the high resistance anti-parallel alignment is defined as Tunnel Magneto-Resistance (TMR). The direction of the reference layer is fixed using an exchange biasing anti-ferromagnetic layer. Writing a bit consists in setting the magnetization direction of the free storage layer using a magnetic field. The basic operation in reading one bit cell is to find the resistance state of the tunnel junction, i.e. the magnetization configuration. The knowledge on spin dependent magnetic tunnel junctions has increased dramatically since 1995 when the first tunnel TMR signals were measured at room temperature [4]. Since then, the evolution observed in tunnel junctions has been enormous, with advances made in the field summarized in some extended reviews [5,6]. Recent breakthroughs in tunnel junction fabrication led to TMR signals close to 70% in CoFeB/AlOx/CoFeB [7] and over 200% [8,9] in junctions with a MgO tunnel barrier. The higher the TMR signals, the greater the separation of the low and high resistance values corresponding to the two bit states. The bit resistance mainly determines the RC time constant and read access time, with typical cell values of 10 kΩ allowing for ns access times [10,11], depending on the lead line capacitance. The characteristic resistance × area product (R × A) is determined by the tunnel barrier height ϕ and thickness t. Resistance dispersion around the central resistance values occurs due to issues in junction patterning, area dimensional control and barrier thickness non-uniformity induced by electrode roughness. It has been shown that it is possible to keep a maximum TMR signal over R×A values ranging from 100–10^6 Ω μm^2 corresponding to AlO_x thickness between 9 Å and 20 Å [12]. Much investigation is being realized for further decreases down to 1 Ω μm^2 keeping full TMR to allow the use of spin transfer induced magnetization reversal to write the bit cell. Bit cell scaling requires also lowering R × A values to keep a constant bit resistance while shrinking the bit cell below the 90 nm node.

2.1. MRAM architectures

Dense MRAM arrays are organized in a 2D matrix with bit elements at each line-column intersection. One bit readout requires a controlled current flow in the matrix in order to correctly address the resistance state of a single element. One method is to use a semiconductor device, either a diode [13] or a transistor [14], in series with the tunnel junction to provide the necessary selectivity (Fig. 1(a)). The two terminal element of the junction-diode matrix makes it the simplest implementation. However, integration with amorphous Si diodes [15] requires large diode areas to source the read current and GaAs diodes are not a mainstream semiconductor technology [16]. Attempts to create a high density cell using a MTJ integrated with a metal/insulator/metal diode showed only poor current densities (0.2 μA/μm^2) and diode rectification ratios of ≈20 [17]. The transistor matrix is the preferred choice because it provides a higher current saturation for the same cell size. The maximum cell current change (i.e. read margin) is obtained when the current flow in the bit element is limited by the resistance of the tunnel junction and not by the transistor saturation current. This is achieved when the junction load curve intercepts the transistor I–V characteristic in the linear region.

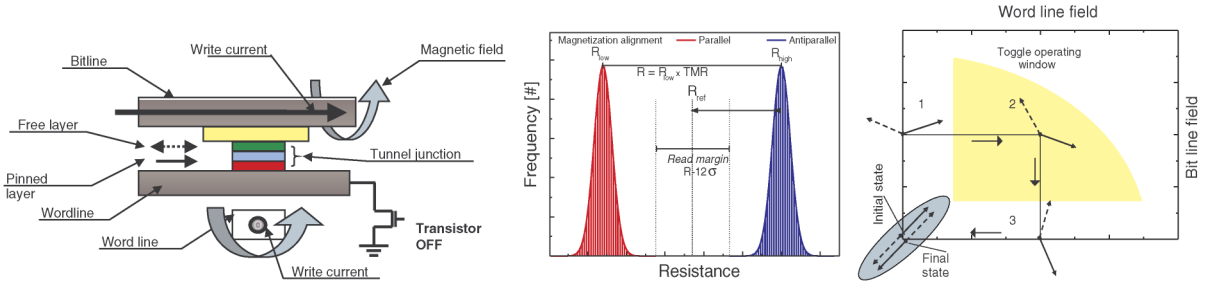

Fig. 1. Elementary MRAM cell (left – a). Distribution of resistance values in tunnel junction array showing the required 12σ read margin (center – b). Toggle switching sequence (right – c).

Another possibility to achieve very high density is to use a matrix design with no semiconductor elements. At the expense of a more elaborated measuring scheme, preventing parasitic current paths, it is possible to accurately measure the resistance of one given tunnel junction in the matrix. One proposed scheme [18] relies on the current measurement circuitry to create a virtual ground. The virtual ground can be created using a operational amplifier with a feedback network, and the current flow can be measured using an inverted amplifier topology. Since all column leads are connected to either the virtual ground or the real ground, the junction voltage drop is set by the bias applied to one of the matrix lines. Other approaches follow the same spirit of controlling the bias voltage of the column and row lines to define unique current paths [19]. The drawbacks are an increased access time due to the time required to establish the necessary voltage levels in the lead lines and a greater design complexity and surface area of the readout circuitry.

2.2. Reading a bit

To assess the bit state the bit resistance is compared to a reference value mid-way between the bit high (R_{high}) and low (R_{low}) resistance values. The inevitable resistance dispersion centered on R_{high} and R_{low} must be reduced since it impacts directly on the read margin. Since the tails of the resistance dispersion must not overlap to be correctly assessed, the available read margin is only $\Delta R - 12\sigma$, where the resistance change ΔR is equal to $R_{\text{low}} \times TMR$ and σ is the dispersion standard deviation. The requirement of a 6σ tail reduces the probability of one bit being outside the $\pm 6\sigma$ interval to 1 in 10^9. A 12σ margin is necessary to accommodate for process drifts and allow the fabrication of large memory sizes. The bit resistance is determined by reading the current flow through the tunnel junction at a fixed voltage. Typical read voltage values are 300 mV, close to the voltage $V_{1/2}$ at which TMR drops to half its maximum low bias value and where maximum current variation is expected.

2.3. Writing a bit

The most widely adopted method to achieve write selectivity in MRAM relies on the Stoner–Wohlfarth theory of coherent rotation in single domain particles. Energy minimization can be used to find that the easy axis field H_e required to reverse the magnetization is reduced by applying simultaneously a second perpendicular field along the hard axis H_h. The solution yields an astroid equation, $H_h^{2/3} + H_e^{2/3} = (2K/M_s)^{2/3}$, where K is the effective anisotropy, accounting for crystalline and shape anisotropies, and M_s the saturation magnetization. Switching occurs for any combination of fields for which the resulting field vector lyes outside the astroid. This allows the selective switching of one bit in the matrix by choosing easy and hard axis fields inside the astroid. This approach has been applied with success to switch individual bits, but dispersion in the switching fields is difficult to control. The reason is that switching fields are mostly determined by shape anisotropy. Small deviations in shape dimensions and edge roughness have a too large influence in the switching field distribution of large bit arrays. Also, a fully single domain behavior cannot be warranted for all bits and domain configurations are not always reproducible. Another issue is the thermal activation of half-selected bits which increases the risk of addressing errors. Finding a set of fields which can be used to program all cells becomes difficult or unusable due to the very narrow operating window [20]. Several approaches have been tried to overcome these problems. One was the use of special bit shapes trying to find reproducible magnetic domain configurations with higher selectivity to the hard axis field, either by using end shape tapering [21,22] and more recently a ‘goggle’ shape [23]. Recent works achieved to reduce vortex formation [24] using a soft adjacent layer of NiFe to provide magnetic flux closure and reduce the demagnetizing field created by the magnetic charges on the storage layer edges. Another proposed solution is the use of synthetic ferrimagnet (SF) storage layers, two ferromagnetic layers coupled anti-ferromagnetically by a Ru spacer, to increase the single domain character [25,26] and reduce sensitivity to shape anisotropy [27].

SF structures have another significant advantage over simple ferromagnetic layers, in that it is possible to reduce the effective magnetization, $M_{\text{eff}} = M_1 - M_2$, without decreasing the total magnetic volume. This is beneficial for the thermal stability of the memory element, since the energy barrier, E_b, between the two possible magnetization configurations of the storage layer is equal to $KV(1 - HM_s/(2K))$. The commonly accepted requirement for 10 year stability is $E_b \geqslant 50\ k_B T$ [28], with $k_B T$ being the thermal energy. Higher margins are required when taking into account that commercial operating temperature range must be specified up to 70 °C and that during write operations half-selected bits are subjected to magnetic fields that reduce the energy barrier E_b. Using SF layers it is possible to increase the effective magnetic volume without increasing the switching field [29,30], however the improvement in thermal stability of non-circular elements is very limited.

2.4. Toggle writing

The toggle approach which was proposed originally by Savtchenko [31], provides a more reproducible magnetization reversal process than the Stoner–Wohlfarth astroid. The toggle write sequence is illustrated in Fig. 1(c). The storage layer is a SF free layer and the current lines generating the field are at 45° with respect to the bit easy axis. For an applied magnetic field higher than the spin-flop field, the SF free layer system minimizes the magnetostatic energy by a scissoring of the two coupled ferromagnetic electrodes and orienting itself perpendicular to the applied field. Detailed analytical treatment of the system can be found in recent publications [32,33]. This property is used in the toggle mode to rotate the SF free layer first perpendicular to the bitline field (1), then perpendicular to the resulting bit and word line field (2), and finally perpendicular to the wordline field (3). When the field is removed the SF layer will orient itself along the bit easy axis, with the magnetization directions of the two ferromagnetic layers of the SF structure reversed compared to their initial orientation. The bit writing sequence now requires the sequential application of the fields created by the current lines with a time overlap of ≈ 5 ns [34]. In toggle writing it is only possible to reverse the initial SF free layer orientation. Therefore, prior to the write process the bit state must be read to determine if a change in bit resistance state is required. This drawback is compensated by the advantage of a single current polarity to create the magnetic field, independently of the bit value being written. This allows the optimization of the CMOS transistors for current sinking or sourcing.

2.5. Current line cladding

In both toggle or astroid approaches a current flow in the electrical leads is used to generate a local magnetic field. A simple expression for the created field is obtained when the current line can be considered as a sheet of current (width $\gg$ thickness), in which case [35] the maximum field value at the center of the line is $I/(2w)$, where I is the current and w the line width. To decrease power consumption with simple lines it is possible to reduce the distance to the sensor or the lateral line dimensions. One other method proposed to increase the created field [36] is using a magnetic cladding layer. The principle is to 'divert' the field generated on the back side of the current line, so that it will add to the field on the bit cell side. The field on back of the line aligns the magnetization of the cladding layer, generating a stray field that adds or subtracts to that of the line depending on the side. The illustrating schematic is shown in Fig. 2(a). Cladding is most effective when the sidewalls and bottom of the current line are covered. The field generated by the cladded line increases by a factor of 2 reaching typical values of 2–10 Oe/mA. It is worth noting that the cladding also acts as a shield against external magnetic fields.

3. New approaches in MRAM

As described in the previous section, the first MRAM generation relies on the superposition of two orthogonal magnetic fields to create the selectivity. The use of the simple Stoner–Wohlfarth astroid as a write selection scheme has to face poor write margins as well as endurance and reliability issues due to the thermal activation of half-selected bits. The toggle approach may be suitable for the two next technological nodes, despite the penalty of a much higher switching energy, but alternative write schemes are necessary beyond the 65 nm node to allow for an appropriate scaling along the ITRS roadmap.

3.1. Thermally assisted MRAM

An alternative write scheme is to assist thermally the switching of the magnetization [37–40]. This approach is based upon the reduction by heating of the required switching fields. There are many possible designs proposed in the literature for the MRAM cell, where the heating method or the thermal dependence of the magnetic properties of the MRAM cell varies: low Curie point design [38], exchange biased storage layer [37,40], perpendicular ferromagnetic layer [41]. Furthermore, the heating is achieved either by passing the current through the sense and/or word lines [38,39] or by sending the current directly through the junction [40].

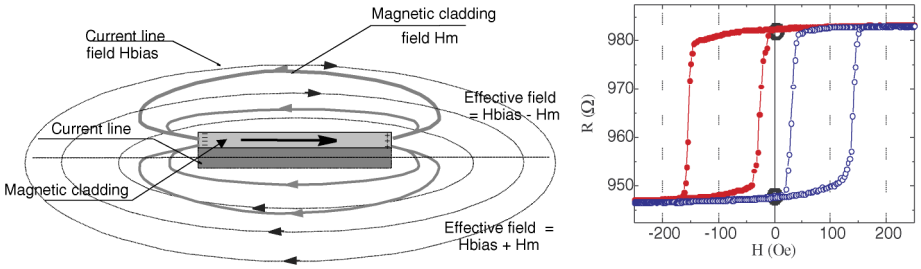

Fig. 2. Diagram of current line cladding (left – a). Demonstration of thermally assisted writing using 20 ns voltage pulse of 2 V and an applied magnetic field of 20 Oe (right – b).

A first design proposed by Daughton and co-workers [38,42] uses a low Curie point ferromagnetic cell with shape anisotropy. The dot can be relatively thick for thermal stability at low temperatures, and can be written with relatively small fields as the dot is cooled through the Curie point. The proposed cell configuration has a heating element, the MRAM bit and an orthogonal digit line that applies a field that determines the state of the bit. The heating element sits above a thin dielectric layer deposited on the silicon substrate that serves as a heat sink. The write current raises the temperature of the heating element slightly above the Curie point of the storage layer. Ferromagnetic magnetization changes very rapidly at temperatures just under the Curie temperature.

In a second design the MTJ stack of the cell is slightly modified: the storage layer comprises a ferromagnetic layer exchange biased by a low blocking temperature (T_B) antiferromagnetic material [40,43,44]. The cell is heated directly by flowing a heating current through the junction during the write procedure. The hot electrons injected through the tunnel barrier relax by emission of phonons and magnons which in turn heat up the storage layer. When the storage layer temperature exceeds T_B, the ferromagnetic layer is freed and can be reversed under the application of a small magnetic field provided by a single digit line. The magnetic field is maintained beyond the heating voltage pulse in order to cool the MTJ under magnetic field and ensure a correct pinning of the storage layer. This write scheme offers many advantages. First, the selectivity is very good as only the selected heated junctions can be written regardless of the external field amplitude (non-heated cells are field immune, due to the exchange bias). Second, the exchange bias storage layer has an increased intrinsic anisotropy due to exchange bias which allows (i) dots with a low aspect ratio down to 1:1 which minimizes the switching field and makes it scaling-independent (ii) thermally stable cells even for small feature sizes and without the need to increase the thickness of the storage layer. Finally, the exchange biasing of the storage layer guarantees a high protection against magnetic erasure (the memory can only be erased by the superposition of a high temperature and a magnetic field). Fig. 2(b) shows the magnetic loops of the storage layer before and after write operation. The loops are clearly shifted from zero field due to the exchange bias on the storage layer. In zero magnetic field, there are two distinct states corresponding to the digital information 0 or 1. The write operation was performed using 20 ns heating voltage pulse of 2 V and a small external magnetic field of 20 Oe. Minimizing the required power density requires adding thermal barriers on each size of the MTJ. These thermal barriers made from a low thermal conductivity material with reasonably low electrical resistivity are very efficient to decrease the heating power density as they help to confine the generated heat in the MTJ. It is important to point out that in this scheme the power density becomes size-independent – an important factor for future scaling.

In order to prevent magnetization curling at the edges of the cell favoring vortex structures the aspect ratio should be larger than 2 for in plane magnetization [45] or to align the magnetization perpendicular to plane. Uniform magnetization distribution can be achieved for rare-earth (RE) and transition metal (TM) compounds given the low saturation magnetization. Since the coercivity of RE-TM alloys strongly depends on temperature, MRAM cells composed of RE-TM alloys [41] may possess high coercivity with stable domain structures at room temperature and meanwhile a small switching field can be achieved by using thermally assisted-writing. The magnetization of the free layer of the giant magnetoresistance films, composed of RE-TM alloys with perpendicular magnetization, can be switched at the field of 10 Oe by heating the sample above the Curie temperature of the free layer.

To conclude this paragraph, the thermally assisted approach offers a promising solution for the next generations of MRAM as it can solve most of the current issues (write selectivity, power consumption, thermal stability) whilst offering full scalability up to the 65 nm node and beyond. Further work on the dynamics of the magneto-thermal switching and durability of the materials under temperature and voltage stress will be required however to further validate this approach.

3.2. Use of precessional switching for ultra-fast MRAMs

To achieve sub-ns write time, several groups have proposed to use precessional switching of magnetization [46–48]. For such precessional switching, fast rising in plane field pulses orthogonal to the initial direction of the magnetization are applied; see

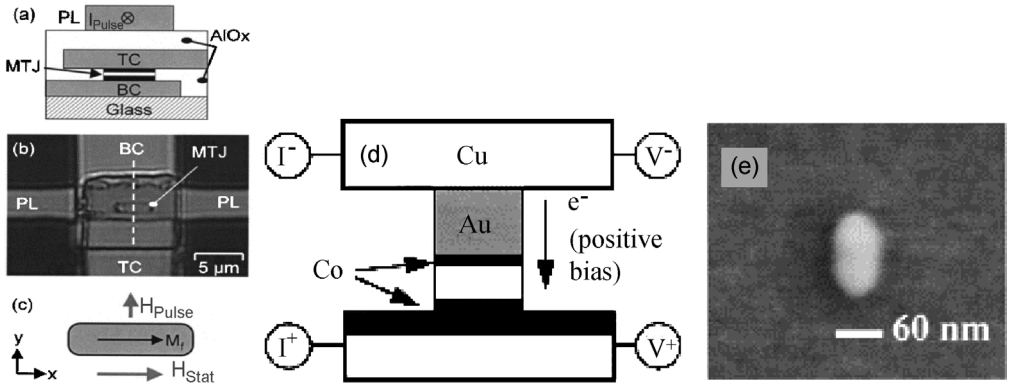

Fig. 3. Sketch of the layer scheme in precessional switching experiments (left – a). Optical micrograph of the device (left – b) and sketch of the magnetic field configuration (left – c). Schematic cross section of the nanopillar (center – d) and micrograph of the Co nanomagnet (right – e).

Fig. 3(a)–(c). These field pulses initiate a large angle precession which can be used to switch the magnetization. Stopping the field pulse when the precessing magnetization is oriented near the reversed easy direction will consequently lead to relaxation towards the reversed direction and thus to magnetization switching. So far precessional switching of soft magnetic cells has been observed on Co based thin films [49], microscopic spin valves [50], permalloy platelets [51] and microscopic magnetic tunnel junctions [52]. For the case of MTJ, reversible switching back and forth of large domains of the free layer magnetization by transverse pulses as short as 170 ps was obtained. The method was in consequence proposed as a way towards efficient, ultrafast, reliable, and energy cost effective precessional switching of the free layer magnetization in MRAMs. Devolder et al. [53] described analytically the magnetization trajectories of a loss-free thin anisotropic macrospin subjected to two orthogonal field pulses. Magnetization switching is known to occur if the fields are above the dynamical astroid, calculated from numerical integration of the Landau–Lifschitz equation. The authors explained that a robust reversal scenario requires a hard-axis field pulse unipolar, short, and fast rising. Conversely, the easy-axis field should be bipolar to select the state to be written and it should be of longer duration with no stringent constraint on its rise and fall times. Their analytical charts are useful to define which sets of field parameters can make reliable precessional switching in MRAM, where other phenomena (intercell dipolar, coupling, magnetic parameter dispersion, etc.) can render the purely numerical optimizations extremely cumbersome. The modest size of the addressing window engenders quite a strong motivation to find technical solutions that minimize the intercell dipolar coupling in dense MRAM arrays. Maunoury et al. [54] implemented direct write and toggle switching in the precessional limit on micron-sized magnetic tunnel junctions, with a combined pulsed hard-axis field and a quasistatic easy-axis field. They measured the amplitudes and duration of orthogonal applied magnetic fields leading to reliable switching for pulse durations as short as 178 ps. Finally, the best field timing was determined in order to maximize the writing operation window. The size of the writing window in two scenarios of orthogonal field timing: synchronous pulses or imbricate pulses (easy-axis field lasting longer than hard-axis field). It was found that imbricate pulses lead to sizeable increase of the writing window. All these results on precessional switching represent certainly a step further to assess the technological potential for ultrafast MRAM applications.

3.3. Current induced magnetic switching MRAM

A novel switching method by spin-polarized current [55,56] has been demonstrated in several recent experiments [57–59]. It is based on the injection of polarized spin current of high densities through a submicron pillar made of normal metal sandwiched between a thin and a thick ferromagnet and works with no applied magnetic field; see Fig. 3(d)–(e). According to most spin transfer models, the thick layer polarizes the spin of the incoming electrons. The polarized current transfers to the local magnetization of the thin layer the transverse part of the spin angular momentum. When the current is sufficiently large, the spin transfer torque can counterbalance the damping term and eventually reverse the thin layer magnetization direction. Applied to MRAMs, the spin induced reversal mechanism could restore the scalability of the cell size beyond several Gbit/chip. However, even if the proof of the concept has been made, some problems still exist. In particular, low switching current density and high read signal are required for the application of the spin induced switching to MRAM. This raises considerable challenges since the MRAM cells must be able to withstand high current densities ($10^7 \mathrm{A/cm^2}$) without exceeding the breakdown voltage of the barrier. Moreover, the write current determines the size of the write transistor, which sets a limit on the memory areal density. Therefore, it is beneficial to lower the resistance of the MTJ [60] or to boost the magnitude of spin torque to enable switching

at lower current [61–63]. Other major concerns are to obtain a fast switching within a few ns and to understand the associated thermal influences on switching [64,65].

Low resistance MTJs have been studied for several years primarily in order to replace the current in-plane read heads for high density magnetic recording [60,66]. As the typical critical current density needed for reversal is as high as 10^6–10^7 A/cm^2, it was important to develop low RA MTJ with high breakdown voltage and high MR ratios for current induced switching MRAM applications [67,68].

Based on the spin-momentum transfer model, the critical current at 0 K is proportional to $M_s V(H_{ext} \pm H_{ani} \pm M_s/2m_0)/g$, where M_s is the saturation magnetization of a magnet cell, V is the volume of the magnetic cell, g corresponds to the efficiency of spin-transfer switching, H_{ext} is the external applied field, H_{ani} is a uniaxial anisotropy field, and $M_s/2m_0$ is half of the anisotropy field in the plane. To decrease the critical current density by more than an order of magnitude, several approaches are possible: decreasing the volume V of the magnetic cell [69], increasing the efficiency g of the spin transfer switching using a double spin filter structure [70] and reducing the saturation magnetization M_s by using a CoFeB magnetic layer [71].

The switching speed scales with $|I - I_C| \ln u_0$, where $I - I_C$ is the overdrive current and u_0 the initial misalignment between the transported spin polarization and the macrospin to be reversed [65]. However, in experiments so far u_0 was the misalignment of the magnetization of the free layer from its easy axis, mostly arising from finite temperature fluctuations. Increasing the switching speed can thus be done by increasing either the current pulse I, which is not desirable or by preparing a more favorable initial condition. A straightforward strategy is to change u_0 by a field pulse transverse to the easy axis, as classically done in magnetic field switching [72]. However in practical memory architectures, this strategy would require additional addressing lines and large transistors to provide enough current, which would significantly increase the technological complexity. A strategy to decrease the current pulse duration needed for a spin-transfer switching event while keeping the full magnetoresistance ratio and not requiring applying any magnetic field was recently proposed [73]. In this approach, the pillar was initially precharged with a dc bias current to excite a steady state precession. In this way, the magnetization is very unlikely to be collinear with the spin of the incoming spins when the write current pulse is sent. The so-prepared precession increases the efficiency of the pulsed current and significantly accelerates the reversal for given current amplitude. Equivalently, it reduces the total current needed to reverse in a certain duration. This strategy was proven efficient for pulse duration between 200 ps and 2 ns, with potential usefulness down to 60 ps.

4. Summary

This article reviews the present state-of-the-art MRAM technology and its perspective evolution. The working principle of conventional cross point architecture based on the Stoner–Wohlfarth selection astroid is described and its main limitations are discussed. New writing procedures proposed recently are presented, including: toggle writing, thermal assisted switching, precessional and the spin transfer induced switching. The advantages/disadvantages of each technology are discussed in terms of thermal stability, selectivity, writing speed and scalability.

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References

[1] S. Tehrani, E. Chen, M. Durlam, M.D. Herrera, J.M. Slaughter, J. Shi, G. Kerszykowski, High density submicron magnetoresistive random access memory, J. Appl. Phys. 85 (1999) 5822.
[2] P.K. Naji, M. Durlam, S. Tehrani, J. Calder, M.F. DeHerrera, A 256 kb 3.0 V 1T1MTJ nonvolatile magnetoresistive RAM, ISSCC Digest of Technical Papers (2001) 122–123.
[3] R. Scheuerlein, A 10 ns read and write non-volatile memory array using a magnetic tunnel junction and a FET switch in each cell, ISSCC Digest of Technical Papers (2000) 128–129.
[4] J.S. Moodera, L.R. Kinder, T.M. Wong, R. Meservey, Large magnetoresistance at room temperature in ferromagnetic thin film tunnel junctions, Phys. Rev. Lett. 74 (1995) 3273.
[5] J.S. Moodera, G. Mathon, Spin polarized tunneling in ferromagnetic junctions, J. Magn. Magn. Mater. (1999) 248–273.
[6] J.S. Moodera, J. Nassar, G. Mathon, Spin tunneling in ferromagnetic junctions, Annu. Rev. Mater. Sci. 29 (1999) 381.
[7] D. Wang, C. Nordman, J.M. Daughton, Z. Qian, J. Fink, 70% TMR at room temperature for SDT sandwich junctions with CoFeB as free and reference layers, IEEE Trans. Magn. 40 (4) (2004) 2269–2271.

[8] S. Yuasa, T. Nagahama, A. Fukushima, Y. Suzuki, K. Ando, Giant room-temperature magnetoresistance in single-crystal Fe/MgO/Fe magnetic tunnel junctions, Nat. Mater. 3 (2004) 868.
[9] S.S. Parkin, C. Kaiser, A. Panchula, P.M. Rice, B. Hughes, M. Samant, S.-H. Yang, Giant tunelling magnetoresistance at room temperature with MgO(100) tunnel barriers, Nat. Mater. 3 (2004) 862.
[10] H. Boeve, J. Das, L. Lagae, P. Peumans, C. Bruynseraede, K. Dessein, L.V. Melo, R.C. Sousa, P.P. Freitas, G. Borghs, J.D. Boeck, Technology assessment for MRAM cells with magnet/semiconductor bits, IEEE Trans. Magn. 35 (1999) 282.
[11] J.M. Daughton, Magnetic tunneling applied to memory, J. Appl. Phys. 81 (1997) 3758–3763.
[12] J.J. Sun, P.P. Freitas, V. Soares, Low resistance spin-dependent tunnel junctions deposited with a vacuum break and RF plasma oxidized, Appl. Phys. Lett. 74 (1999) 448–450.
[13] W.J. Gallagher, J. Kaufman, S. Parkin, R. Scheuerlein, Magnetic memory array using magnetic tunnel junction devices in the memory cells, U.S. Patent 5640343, June 1997.
[14] M. Durlam, S. Tehrani, J. Calder, M.F. DeHerrera, P.K. Naji, Non volatile RAM based on magnetic tunnel junction elements, ISSCC Digest of Technical Papers (2000) 130–131.
[15] R.C. Sousa, P.P. Freitas, V. Chu, J.P. Conde, Vertical integration of a spin dependent tunnel junction with an amorphous Si diode, Appl. Phys. Lett. 74 (1999) 3893.
[16] H. Boeve, R.C. Sousa, P.P. Freitas, J.D. Boeck, G. Borghs, Electrical characteristics of magnetic memory cells comprising magnetic tunnel junctions and GaAs diodes, Electron. Lett. 36 (21) (2000) 1782–1783.
[17] C. Tiusan, M. Chshiev, A. Iovan, V. da Costa, D. Stoeffler, T. Dimopoulos, K. Ounadjela, Quantum coherent transport versus diode-like effect in semiconductor-free metal/insulator structure, Appl. Phys. Lett. 79 (25) (2001) 4231–4233.
[18] F.Z. Wang, Diode-free magnetic random access memory using spin-dependent tunneling effect, Appl. Phys. Lett. 77 (13) (2000) 2036–2038.
[19] Y. Zheng, X. Wang, D. You, Y. Wu, Switch-free read operation design and measurement of magnetic tunnel junction magnetic random access memory arrays, Appl. Phys. Lett. 79 (17) (2001) 2788–2790.
[20] M. Yoshikawa, T. Kai, M. Amano, E. Kitagawa, T. Nagase, M. Nakayama, S. Takahashi, T. Ueda, T. Kishi, K. Tsuchida, S. Ikegawa, Y. Asao, H. Yoda, Y. Fukuzumi, K. Nagahara, H. Numata, H. Hada, N. Ishiwata, S. Tahara, Bit yield improvement by precise control of stray fields from SAF pinned layers for high-density MRAMs, J. Appl. Phys. 97 (10) (2005) 10P508.
[21] J. Gadbois, J.-G. Zhu, W. Vavra, A. Hurst, The effect of end and edge shape on the performance of pseudo-spin valve memory cells, IEEE Trans. Magn. 34 (4) (1998) 1066–1068.
[22] M. Redjdal, P.W. Gross, A. Kazmi, F.B. Humphrey, Switching dependence on fabrication accuracy of tapered ends of a single giant magnetoresistance memory cell in word disturb condition, J. Appl. Phys. 85 (1999) 6193–6195.
[23] S.C. Oh, J.E. Lee, H.-J. Kim, Y.K. Ha, J.S. Bae, K.T. Nam, E. Kim, S.O. Park, H.S. Kim, U.-I. Chung, J.T. Moon, Improvement of writing margin in MRAM with novel shape, J. Appl. Phys. 97 (10) (2005) 10P509.
[24] Y. Guo, P. Wang, M.-M. Chen, C. Horng, T. Min, L. Hong, O. Voegeli, R. Tong, P. Chen, S. Le, J. Chen, T. Zhong, L. Yang, G. Liu, Y. Chen, S. Shi, K. Yang, D. Tsang, MRAM array with coupled soft-adjacent magnetic layer, J. Appl. Phys. 97 (10) (2005) 10P506.
[25] K. Inomata, N. Koike, T. Nozaki, S. Abe, N. Tezuka, Size-independent spin switching field using synthetic antiferromagnets, Appl. Phys. Lett. 82 (16) (2003) 2667–2669.
[26] K. Inomata, T. Nozaki, N. Tezuka, S. Sugimoto, Magnetic switching field and giant magnetoresistance effect of multilayers with synthetic antiferromagnet free layers, Appl. Phys. Lett. 81 (2) (2002) 310–312.
[27] W.C. Jeong, J.H. Park, G.H. Koh, G.T. Jeong, H.S. Jeong, K. Kim, Switching field distribution in magnetic tunnel junctions with a synthetic antiferromagnetic free layer, J. Appl. Phys. 97 (10) (2005) 10C905.
[28] N.D. Rizzo, M. DeHerrera, J. Janesky, B. Engel, J. Slaughter, S. Tehrani, Thermally activated magnetization reversal in submicron magnetic tunnel junctions for magnetoresistive random access memory, Appl. Phys. Lett. 80 (13) (2002) 2335–2337.
[29] J. Janesky, N.D. Rizzo, B.N. Engel, S. Tehrani, The switching properties of patterned synthetic ferrimagnetic structures, Appl. Phys. Lett. 85 (12) (2004) 2289–2291.
[30] Y. Saito, H. Sugiyama, K. Inomata, Thermal stability parameters in synthetic antiferromagnetic free layers in magnetic tunnel junctions, J. Appl. Phys. 97 (10) (2005) 10C914.
[31] L. Savchenko, B.N. Engel, N.D. Rizzo, M.F.D. Herrera, J.A. Janesky, U.S. Patent No. 6,545,906, April 2003.
[32] D.C. Worledge, Spin flop switching for magnetic random access memory, Appl. Phys. Lett. 84 (22) (2004) 4559–4561.
[33] H. Fujiwara, S.-Y. Wang, M. Sun, Critical-field curves for switching toggle mode magnetoresistance random access memory devices (invited), J. Appl. Phys. 97 (10) (2005) 10P507.
[34] T. Yamamoto, H. Kano, Y. Higo, K. Ohba, T. Mizuguchi, M. Hosomi, K. Bessho, M. Hashimoto, H. Ohmori, T. Sone, K. Endo, S. Kubo, H. Narisawa, W. Otsuka, N. Okazaki, M. Motoyoshi, H. Nagao, T. Sagara, Magnetoresistive random access memory operation error by thermally activated reversal (invited), J. Appl. Phys. 97 (10) (2005) 10P503.
[35] T.J. Silva, C.S. Lee, T.M. Crawford, C.T. Rogers, Inductive measurement of ultrafast magnetization dynamics in thin-film permalloy, J. Appl. Phys. 85 (11) (1999) 7849–7861.
[36] E. Chen, S. Tehrani, M. Durlam, T. Zhu, Magnetic memory and method therefor, U.S. Patent 5659499, August 1997.
[37] J. Wang, P.P. Freitas, Low-current blocking temperature writing of double barrier magnetic random access memory cells, Appl. Phys. Lett. 84 (6) (2004) 945–947.
[38] J.M. Daughton, A.V. Pohm, Design of Curie point written magnetoresistance random access memory cells, J. Appl. Phys. 93 (10) (2003) 7304–7306.
[39] R.I. Waite, A.V. Pohm, C.S. Comstock, Thermal noise limitations to $2 \times 20\ \mu m^2$ magnetoresistive memory element thresholds, J. Appl. Phys. 63 (8) (1988) 3151–3152.

[40] I.L. Prejbeanu, W. Kula, K. Ounadjela, R.C. Sousa, O. Redon, B. Dieny, J.-P. Nozières, Thermally assisted switching in exchange-biased storage layer magnetic tunnel junctions, IEEE Trans. Magn. 40 (4) (2004) 2625–2627.
[41] C.-H. Lai, Z.-H. Wu, C.-C. Lin, P.H. Huang, Thermally assisted-writing giant magnetoresistance with perpendicular magnetization, J. Appl. Phys. 97 (10) (2005) 10C511.
[42] R.S. Beech, J.A. Anderson, A.V. Pohm, J.M. Daughton, Curie point written magnetoresistive memory, J. Appl. Phys. 87 (9) (2000) 6403–6405.
[43] R.C. Sousa, I.L. Prejbeanu, D. Stanescu, B. Rodmacq, O. Redon, B. Dieny, J. Wang, P.P. Freitas, Tunneling hot spots and heating in magnetic tunnel junctions, J. Appl. Phys. 95 (11) (2004) 6783–6785.
[44] M. Kerekes, R.C. Sousa, I.L. Prejbeanu, O. Redon, U. Ebels, C. Baraduc, B. Dieny, J.-P. Nozières, P.P. Freitas, P. Xavier, Dynamic heating in submicron size magnetic tunnel junctions with exchange biased storage layer, J. Appl. Phys. 97 (10) (2005) 10P501.
[45] E. Girgis, J. Scheltem, J. Sci, J. Janesky, S. Tehrani, H. Goronkin, Switching characteristics and magnetization vortices of thin-film cobalt in nanometer-scale patterned arrays, Appl. Phys. Lett. 76 (25) (2000) 3780–3782.
[46] C.H. Back, R. Allenspach, W. Weber, S.S.P. Parkin, D. Weller, E.L. Garwin, H.C. Siegmann, Minimum field strength in precessional magnetization reversal, Science 285 (6) (1999) 864.
[47] Y. Acreman, C.H. Back, M. Buess, D. Pescia, V. Pokrosky, Bifurcation in precessional switching, Appl. Phys. Lett. 79 (2001) 2228–2230.
[48] T. Gerrits, H.A.M. van den Berg, J. Hohlfeld, L. Bär, T. Rasing, Ultrafast precessional magnetization reversal by picosecond magnetic field pulse shaping, Nature (London) 418 (2002) 509–512.
[49] M. Bauer, J. Fassbender, B. Hillebrands, R.L. Stamps, Switching behavior of a stoner particle beyond the relaxation time limit, Phys. Rev. B 61 (5) (2000) 3410–3416.
[50] S. Kaka, S.E. Russek, Precessional switching of submicrometer spin valves, Appl. Phys. Lett. 80 (16) (2002) 2958–2960.
[51] H.W. Schumacher, C. Chappert, R.C. Sousa, P.P. Freitas, J. Miltat, Quasiballistic magnetization reversal, Phys. Rev. Lett. 90 (2003) 017204–017207.
[52] H.W. Schumacher, C. Chappert, R.C. Sousa, P.P. Freitas, J. Miltat, J. Ferré, Precessional switching of the magnetization in microscopic tunnel junctions (invited), J. Appl. Phys. 93 (10) (2003) 7290–7294.
[53] T. Devolder, C. Chappert, Cell writing selection when using precessional switching in a magnetic random access memory, J. Appl. Phys. 95 (4) (2004) 1933–1941.
[54] C. Maunoury, T. Devolder, C.K. Lim, P. Crozat, C. Chappert, J. Wecker, L. Bär, Precessional direct-write switching in micrometer-sized magnetic tunnel junctions, J. Appl. Phys. 97 (2005) 074503–074508.
[55] J. Slonczewski, Current-driven excitation of magnetic multilayers, J. Magn. Magn. Mater. 159 (1–2) (1996) L1–L7.
[56] L. Berger, Emission of spin waves by a magnetic multilayer traversed by a current, Phys. Rev. B 54 (1996) 9353.
[57] F.J. Albert, J.A. Katine, R.A. Buhrman, D.C. Ralph, Spin-polarized current switching of a Co thin film nanomagnet, Appl. Phys. Lett. 77 (23) (2000) 3809–3811.
[58] J. Grollier, V. Cros, A. Hamzic, J.M. George, H. Jaffrès, A. Fert, G. Faini, J.B. Youssef, H. Legall, Spin-polarized current induced switching in Co/Cu/Co pillars, Appl. Phys. Lett. 78 (23) (2001) 3663.
[59] J.A. Katine, F.J. Albert, R.A. Buhrman, E.B. Myers, D.C. Ralph, Current-driven magnetization reversal and spin-wave excitations in Co/Cu/Co pillars, Phys. Rev. Lett. 84 (14) (2000) 3149–3152.
[60] Y. Huai, F. Albert, P. Nguyen, M. Pakala, T. Valet, Observation of spin-transfer switching in deep submicron-sized and low-resistance magnetic tunnel junctions, Appl. Phys. Lett. 84 (2004) 3118–3120.
[61] L. Berger, Multilayer configuration for experiments of spin precession induced by a dc current, J. Appl. Phys. 93 (2003) 7693–7695.
[62] K. Yagami, A.A. Tulapurkar, A. Fukushima, Y. Suzuki, Estimation of thermal durability and intrinsic critical currents of magnetization switching for spin-transfer based magnetic random access memory, J. Appl. Phys. 97 (10) (2005) 10C707.
[63] Y. Jiang, T. Nozaki, S. Abe, T. Ochiai, A. Hirohata, N. Tezuka, K. Inomata, Substantial reduction of critical current for magnetization switching in an exchange-biased spin valve, Nat. Mater. 3 (2004) 361–364.
[64] A.A. Tulapurkar, T. Devolder, K. Yagami, P. Crozat, C. Chappert, A. Fukushima, Y. Suzuki, Subnanosecond magnetization reversal in magnetic nanopillars by spin angular momentum transfer, Appl. Phys. Lett. 85 (2004) 5358–5360.
[65] J.Z. Sun, Spin-current interaction with a monodomain magnetic body: A model study, Phys. Rev. B 62 (2000) 570–578.
[66] J. Wang, P.P. Freitas, E. Snoeck, Low-resistance spin-dependent tunnel junctions with $ZrAlO_x$ barriers, Appl. Phys. Lett. 79 (27) (2001) 4553–4555.
[67] Y. Jiang, S. Abe, T. Ochiai, T. Nozaki, A. Hirohata, N. Tezuka, K. Inomata, Effective reduction of critical current for current-induced magnetization switching by a Ru layer insertion in an exchange-biased spin valve, Phys. Rev. Lett. 92 (2004) 167204–167207.
[68] H. Meng, J. Wang, Z. Diao, J.-P. Wang, Low resistance spin-dependent magnetic tunnel junction with high breakdown voltage for current-induced-magnetization-switching devices, J. Appl. Phys. 97 (10) (2005) 10C926.
[69] E.B. Myers, F.J. Albert, J.C. Sankey, E. Bonet, R.A. Buhrman, D. Ralph, Thermally activated magnetic reversal induced by a spin-polarized current, Phys. Rev. Lett. 89 (2002) 196801–196804.
[70] K. Yagami, A.A. Tulapurkar, A. Fukushima, Y. Suzuki, Low-current spin-transfer switching and its thermal durability in a low-saturation-magnetization nanomagnet, Appl. Phys. Lett. 85 (23) (2004) 5634–5636.
[71] H. Kano, K. Bessho, Y. Higo, K. Ohba, M. Hashimoto, T. Mizuguchi, M. Hosomi, MRAM with improved magnetic tunnel junction material, in: INTERMAG Europe 2002, Digest of Technical Papers (2002) BB4.
[72] B.C. Choi, M. Belov, W.K. Hiebert, G.E. Ballentine, M.R. Freeman, Ultrafast magnetization reversal dynamics investigated by time domain imaging, Phys. Rev. Lett. 86 (2001) 728–731.
[73] T. Devolder, C. Chappert, P. Crozat, A. Tulapurkar, Y. Suzuki, J. Miltat, K. Yagami, Precharging strategy to accelerate spin-transfer switching below the nanosecond, Appl. Phys. Lett. 86 (2005) 062505–062507.