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Ultimate lithography/Lithographie ultime

Direct write lithography: the global solution for R&D and manufacturing

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Abstract

The electron beam lithography is a well known and mature solution, widely installed in research laboratories and Universities, to provide advanced patterning for research and development programs for a large field of applications. However, limited by its low throughput capabilities, the direct write solution never appeared as a credible option for manufacturing purposes. Nevertheless, semiconductor business starts to be affected by the increasing cost of the optical lithography requesting more and more complex masks and projection systems. This trend opens opportunities for high throughput mask less equipments to address ASIC manufacturing. A review of the Maskless Lithography (ML2) technology is presented in this article, including process integration capability, application fields and perspective for high throughput ML2 solution. ***To cite this article: L. Pain et al., C. R. Physique 7 (2006).***

Résumé

La lithographie par écriture directe : solution globale pour la R&D et la production. La lithographie par faisceau d'électrons est une solution technologique bien connue, mature et très utilisée dans les laboratoires de recherche et universités qui permet de réaliser des structures avancées pour des programmes de recherche et développement, couvrant un large champ d'applications. Cependant, du fait de sa lenteur d'écriture, la lithographie à écriture directe n'est jamais apparue comme une solution crédible pour la production. Néanmoins, l'accroissement des coûts de la lithographie optique liés à l'utilisation de masques et de systèmes d'exposition de plus en plus complexes, commence à toucher le marché des semi-conducteurs. Cette tendance ouvre des perspectives pour des machines de lithographie sans masque à fort débit pour la production de circuits spécifiques (ASIC). Une revue de la lithographie sans masque (ML2) est présentée dans cette publication, incluant la capacité d'intégration de cette solution, ses domaines d'application ainsi que les perspectives concernant des solutions ML2 à fort débit. ***Pour citer cet article : L. Pain et al., C. R. Physique 7 (2006).***

Keywords: Lithography; E-beam; Direct write; Prototyping

Mots-clés : Lithographie ; Faisceau d'electron ; Écriture directe ; Prototypage

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1. Introduction

The first Electron Beam Lithography (EBL) systems, based on the Scanning Electron Microscope (SEM), were developed in the late 1960s. Since its introduction, EBL has been widely used in research laboratories and Universities because it is capable of very high resolution and it is a very flexible technique. Nevertheless, these systems based on a single Gaussian beam are orders of magnitude slower than optical lithography, making them unsuitable for production. During the 1970s, IBM pioneered the concept of shaped beams, increasing significantly the throughput and leading the industry in the development and application of high-throughput e-beam direct-write systems. In the mean time, interest for this technology decreased due to its higher Cost of Ownership (CoO) compared to the optical lithography one. In the late 1990s, Maskless Lithography (ML2), as it is now more commonly named, regained momentum, because both the cost and cycle time of masks are steadily increasing at each technological node. In attempts to resolve these issues Maskless Lithography approaches are now foreseen for low and medium-volume production.

2. The interest of ML2 lithography

2.1. The different direct write technology solutions

Direct write is a technology allowing direct transfer of patterns onto the wafer. Different writing strategies have been investigated depending of the trade off between resolution and throughput.

Thermoionic or field emission electron guns are the most commonly used sources for direct write applications. Electronic optics using both electromagnetic and electrostatic lenses and coils for beam focalisation and control are well known and mature technologies. Furthermore, because of the short electron wave length, e-beam writing is not diffraction, limited allowing resolution down to the nanometre range.

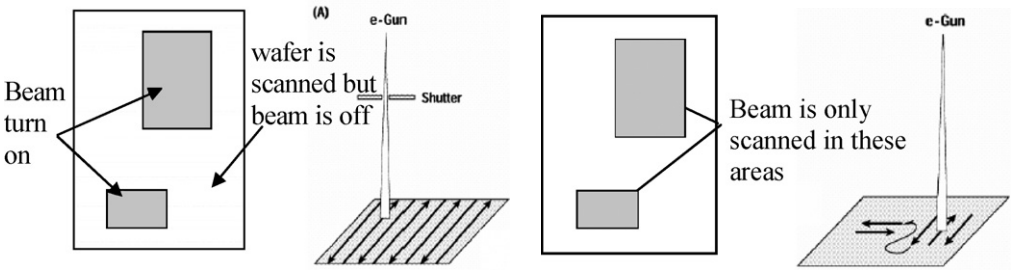
2.1.1. The Gaussian beam raster scan and vector scan

The first Gaussian beam raster scan equipment has been developed by Bell Labs [1] and it is derived from the Cathode Ray Tube (CRT) and Scanning Electron Microscopy (SEM) technologies. The beam is scanned along a line while the stage is continuously moved in the perpendicular direction. The beam is then turned on and off (blanked) along the line according to the pattern to be written. The raster scan strategy requires that pattern data been transformed into a bit map thus producing a huge volume of data to be supplied to the blanker. The throughput of a raster scan is controlled by the frequency (typically 50 MHz) at which the bits can be transmitted to the blanker (data rate) and the minimum exposure time per pixel (dwell time) (Fig. 1(a)).

Other approach consists to scan the electron beam only over the areas that need to be exposed. This is the so called vector scanning. By only addressing the exposed areas this approach has the potential to reduce the writing time. Gaussian beam systems used for direct write application are today using this strategy (Fig. 1(b)).

2.1.2. The shaped beam and Cell Projection

In a shaped beam system each figure is fractured into small shape features called ‘flashed’. These flashed are produced by the image formed by the intersection of two shaped apertures. Different beam shapes can be formed by overlapping two apertures as 90 and 45 degrees rectangles or triangles (Fig. 2). The combination of shaped beam and



(a) Raster scan (b) Vector scan

Fig. 1. Dual scanning configuration for Gaussian beam technology.

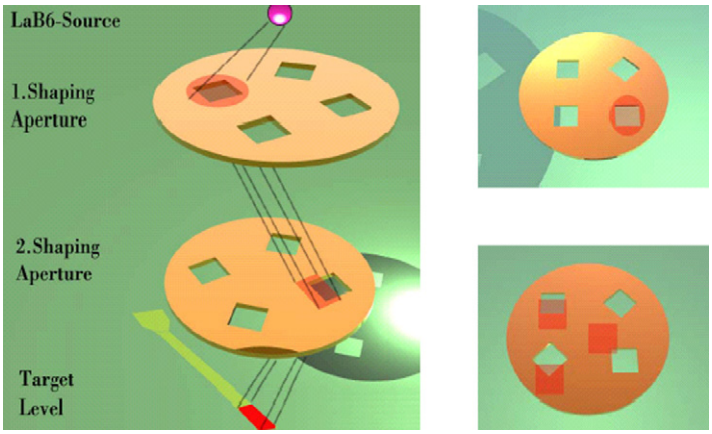


Fig. 2. Principle of the shaped beam.

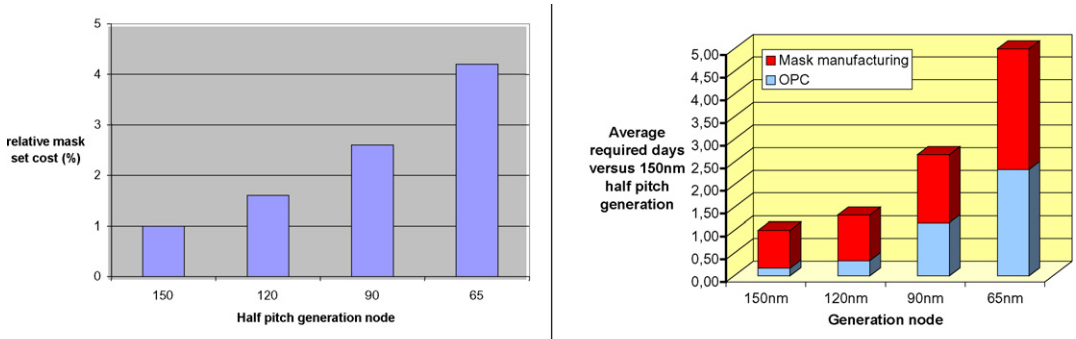
vector scan writing strategy, improve significantly the throughput of the systems, providing a better solution for direct write applications.

Another further step is to be able to print in one shot a part of the circuit which has been identified as a repetitive structure; this is the so-called cell projection. A memory cell, for example, can be duplicated in a cell aperture and then printed in one step, increasing significantly the throughput. Of course, this writing strategy will be only efficient if the circuit to be printed contains a significant amount of such repetitive structures.

2.2. *The opportunities for semiconductor manufacturing*

Since the introduction of the 150 nm half pitch technology node, the contribution of the lithography operations to the overall wafer cost rises steadily at the introduction of each new generation product. The lithography ratio reaches 40% of the cost of a production flow for the 130 nm half pitch generation node [2].

Two main reasons explain such a trend. First, optical scanners need to be improved with new wavelength introduction, very large numerical aperture and the introduction of the latest immersion principle. In addition, the implementation of complex resolution enhancement technique for optical proximity effect control significantly impacts manufacturing budget by increasing mask price and manufacturing cycle time. Figs. 3(a) and (b) highlight this trend on mask cost and cycle time for each new generation node, compared to the 150 nm half pitch generation. These graphs show that mask set price and cycle time have been multiplied respectively by a factor of 4.2 and 6 from 150 to 65 nm half pitch generation. In this context, the use of high throughput maskless systems may represent a



(a) Mask cost trend (b) Mask manufacturing cycle time

Fig. 3. Optical mask cost and cycle time evolution versus technology node insertion.

Table 1
Manufacturing parameters for ML2 usage

Fab. capability	ML2 tool key parameters	Technology insertion
10 000 wafers out per week ML2 usage 10% volume dedicated to → prototyping (10 wafers per lot) → Low runners: 500 wafer/mask	Cost: 10 to 30 M$ Throughput: 20 wafers per hour	45 nm half pitch All critical levels in replacement of EUV of VHNA immersion scanners → 10 layers Mask cost savings: 60%

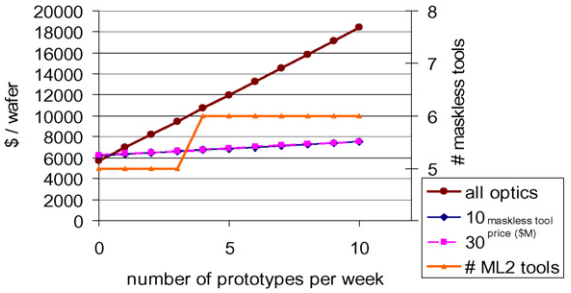


Fig. 4. ML2 cost of ownership presentation and tool number needs for manufacturing in respect to Table 1 scenario.

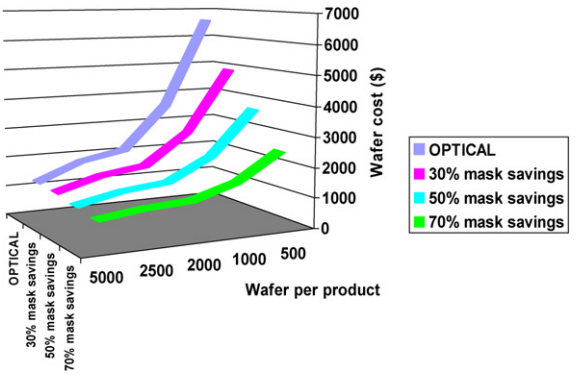


Fig. 5. Impact of mask saving on ML2 profitability.

viable alternative to reduce manufacturing cost by mask budget reduction, especially in the case of ASIC makers and foundries.

Taking into account throughput and tool cost estimation, profitability calculation can be envisioned [3]. Table 1 presents one business case for ML2 insertion at 45 nm half pitch technology. ML2 tools are used for critical level patterning and their usages are forecasted to produce a limited ratio of the full wafer fab capability (10%) for prototyping application. Based on these hypotheses, Fig. 4 shows the cost per wafer evolution in function of the number of prototypes started per week. This graph fully validates the ML2 business opportunity, as up to 66% of the entire lithographic cost can be saved. Moreover, in this scenario, the number of tools looks reasonable. In fact, this profitability depends strongly of the mask cost savings. Fig. 5 details ML2 cost reduction versus various mask savings ratios. With the increase of the mask budget perspectives, the ML2 solution becomes attractive. This is especially the case in the first years of a new technology introduction where masks are the most expensive.

Similar business studies have been performed and published these last years by different organizations and companies [4,5]. The conclusions are very close to the results presented in these graphs. They confirm that the direct write lithography is no longer only a solution for R&D purposes, but also a viable and economical option for semiconductor manufacturing applications.

3. Process integration adaptability of direct write lithography

The use of direct write for wafer manufacturing requires the integration of the lithography processes into the standard CMOS technological flow. This issue implies a full compatibility of the resist process, the alignment strategy and an accurate control of proximity effects. Important developments have been performed at CEA–LETI and Crolles2 Alliance sites to transparently insert a direct write solution for the delivery of wafers in respect of production standards. This paragraph details the results related to this integration work.

3.1. Alignment concern

The overlay performance is a key parameter for process integration and final product functionality. EBDW alignment strategy has also to follow the manufacturing standards where alignment is performed on various ‘reference’

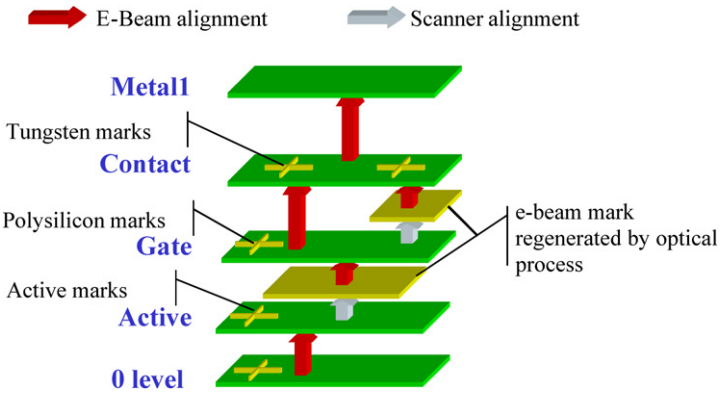


Fig. 6. EBDW alignment strategy overview.

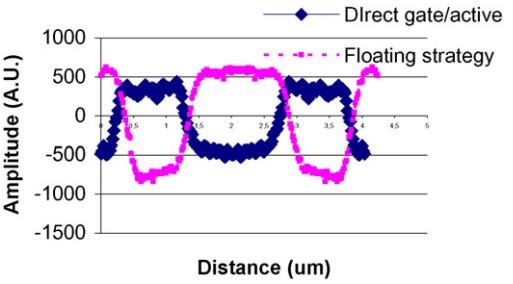


Fig. 7. Chip mark alignment backscattered signal recorded at 50 kV.

levels, as shown on Fig. 6. However, the present e-beam platforms perform alignment directly through the beam by using a back scattered electron detector. The main issue with this solution is its destructive impact by exposing the resist during mark detection. Thus marks can be used only once. In addition to this first concern, accurate mark detection requires a good contrast. For this sufficient topographical step height or local atomic difference is needed.

Alignment strategy is strongly dependent of the stack composition. For contact and all Back End Of Line (BEOL) reference levels, the presence of metallic materials like tungsten, copper allows an alignment solution based on the atomic contrast principle. It is the same principle for the levels aligned on the gate, where the salicide process incorporates metallic compounds into the polysilicon mark generated at gate level, such as cobalt or nickel. Finally, the most difficult situation is to perform alignment on ACTIVE levels. In this case, technological stack composition contents equivalent atomic weight materials and topographical contrast is low due to the planarization process for the realization of shallow trench isolation. However, the oxide over-polishing can create a sufficient recess for topographical read. This recess can be locally amplified by reversing mark polarity design to increase silicon area versus oxide. Fig. 7 presents a record of an active mark done for a gate alignment. As shown on this graph, the signal is large enough to directly align the gate level on the active level.

In the case of lack of mark detection when the topography step is too small, an alternative solution, called the floating strategy, is presented in Fig. 6. Specific alignment marks can be re-generated by optical lithography and transferred into substrate to create topographical contrast. However, with this strategy, the final overlay result is directly dependent of the alignment performance of this additional level. It is a logically degraded versus a direct alignment approach [6]. Nevertheless, this back-up solution is essential as it offers a permanent alignment solution whatever the situation.

These studies showed that in most cases, a direct alignment on a reference level can be achieved. This result confirms that an alignment strategy equivalent to optical scanner can be developed for EBDW lithography. This is a key point for its insertion into technological flow. One example of alignment performance on a Crolles2 lot is presented in Fig. 8. By using optimal writing conditions, a repeatable overlay range value of 36 nm can be reached from lot to lot. Such an overlay value is in accordance with the 90 nm half pitch generation and reaches the specification limits of the 65 nm half pitch generation. However, the VISTEC SB350DW platform with which were obtained the overlay results has been designed in early 2000. A new generation platform with improved stage accuracy and a lower electronic noise is now mandatory to push the overlay capabilities of these systems to fully comply the ITRS targets for the next generations. The implementation of an optical scanner-like solution would be also preferable for this new EBDW generation tool in order to solve the mark alteration issue and also to be able to use the same standard optical mark available in the product periphery.

3.2. Resist processes for high resolution

Different types of resists can be used for e-beam lithography depending of the application, the resolution and process integration requirements (Fig. 9).

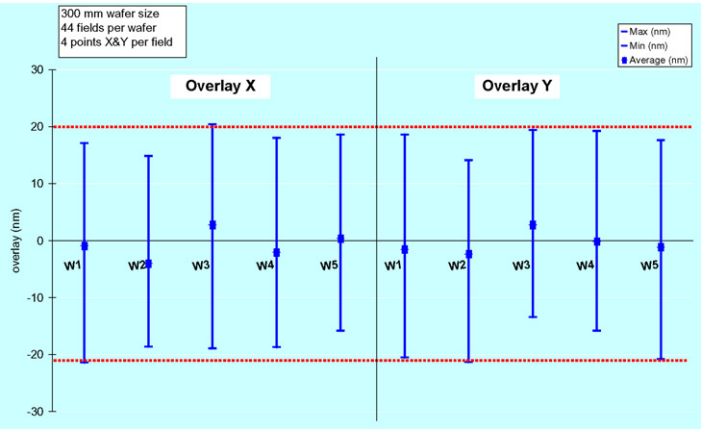


Fig. 8. Overlay results (contact/gate) on electrical lot.

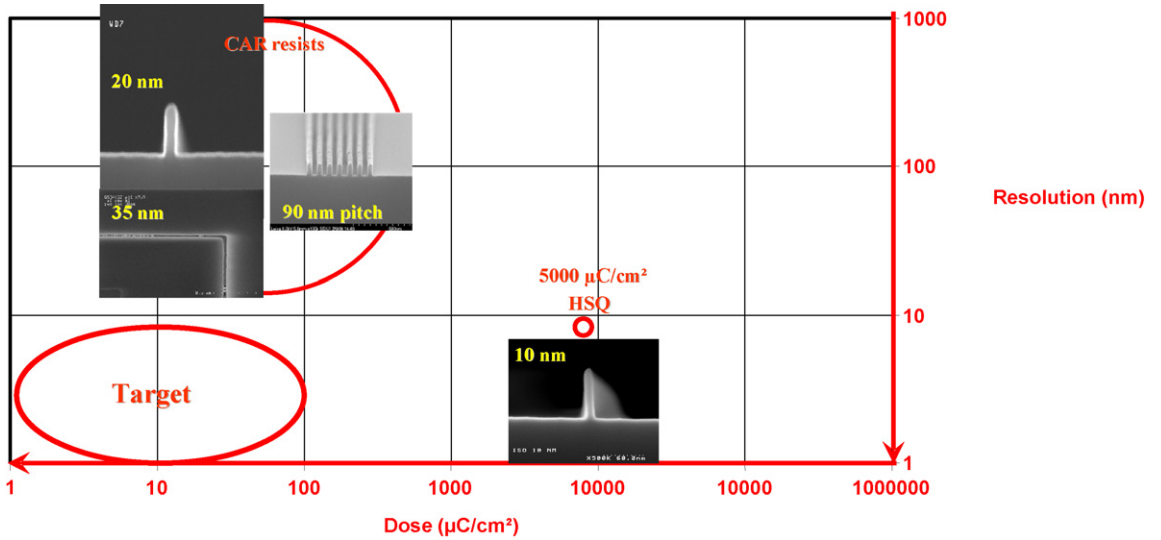


Fig. 9. Resist platform overview for EBDW lithography.

3.2.1. Non Chemically Amplified Resist

Very high resolution can be achieved using non Chemically Amplified Resist. These resists, which can be organic or inorganic, are directly modified by the primary beam of electrons. The main drawback for these resists: is the lack of sensitivity requiring often doses greater than 1 C/cm^2.

Traditionally PMMA (PolyMethyl MethAcrylate) and its co-polymer have been used for very high resolution e-beam lithography. This positive tone resist family, which has shown the best resolution ever achieved by e-beam [7] has a main drawback, in top of the lack of sensitivity, it has a poor etch resistance, and only a liftoff process can be used which is not compatible with CMOS manufacturing.

Calixarene derivatives have been used as a high-resolution negative resist under an electron beam lithography process [8]. Due to their phenolic structure, they show a good resistance to dry etching process but Calixarene resists are low sensitivity resists in the range of few mC/cm^2 which is one order of magnitude less sensitive than PMMA. Another technique for producing nanometer-scale patterns using doses on the order of 1 C/cm^2 is the use of metal fluorides. A high current density of electrons causes the dissociation of materials such as AlF_3 and MgF_2.

Recently an increasing interest has been attributed to HSQ (Hydrogene SilsesQuioxane). This material, used in microelectronic for its dielectric properties, has a three-dimensional framework allowing high resolution whose sensitivity is in the range of PMMA [9,10]. SiH bonds in HSQ are broken under electron-beam irradiation, and then the

crosslinking required for negative tone patterning is generated. HSQ resist is developed in a standard 0.21 normality TetraMethyl Hydroxyl Ammonium (TMAH) developers making him totally compatible with usual processes. Furthermore, a post hard bake induces structural modifications into HSQ which turns into SiO_2 allowing it to be used as a hard mask [11] for lithography process in MOSFET device development.

Finally, molecular resists have been investigated. Such resists as triphenylene and fullerene derivatives use small carbon rich molecules, which offer a good potential for very high resolution, etch resistance and low Line Edge Roughness. To overcome the sensitivity issue, the addition of chemical amplification functionalities is under development. Adding epoxide crosslinker and photoinitiator have increased the sensitivity to electron around 10 $\mu C/cm^2$ [12].

3.2.2. Chemically Amplified Resist (CAR)

Chemically amplified platforms are employed traditionally for semiconductor applications: mask and direct write. These resists based on PHS type polymer, fully suitable for e-beam lithography, are well known and widely used for 248 nm optical lithography. Available in positive and negative tone polarities, they are compatible with semiconductor manufacturing standards: full process integration capabilities (etch, implant), spin coating compatibility, good resist sensitivity (1–100 $\mu C/cm^2$) [13,14]. If the present platform shows a process compatibility for the 45 nm half pitch, technology development requires pushing simultaneously resolution for the next generation node and sensitivity for throughput aspect. However, this trade off is difficult to achieve if we refer to recent work presented at last EIPBN conference on resist process, exploring the impact of resist sensitivity on process window and roughness [15].

To resolve a 70 nm dense lines structure of a metal level exposure, results show that it is necessary to increase the number of electrons per shot to satisfy the Line Edge Roughness (LER) requirement. If present resist platforms with a sensitivity of 10 to 30 $\mu C/cm^2$ succeed to resolve this feature, LER value, around 15 nm, is far from the ITRS target set at 2.4 nm for 65 nm half pitch. Curve extrapolation in this context predicts that a minimum of 7500 electrons is required to properly answer to the LER criteria instead of 1500 electrons (Fig. 10). The present results have been extracted in the Crolles2 configuration with a second generation EBDW system: it highlights the complexity of future chemically amplified resist to meet the ITRS targets. Finally, further developments are mandatory to keep e-beam direct write processes well ahead of optical ones to address manufacturing concerns. First, on resist platform, resist suppliers have to provide new chemistry with higher resolution and contrast properties. Then, on tool aspect, tool manufacturer needs to improve tool performance with low beam blur and improved electronic stability.

3.3. The control of proximity effects

CD control for e-beam lithography is strongly depending on feature dimension and density. This is due to the so call proximity effects. The proximity effects are the result of scattered electrons due to their various potential interactions between electron–electron, electron–resist and electron–substrate. The first interaction, electron–electron or Coulomb interaction, is the result of the spreading of the beam itself, called the ‘blur effect’, enlarging the incident beam. The latter phenomena are due to the interaction between the electron beam and the atoms of the resist and

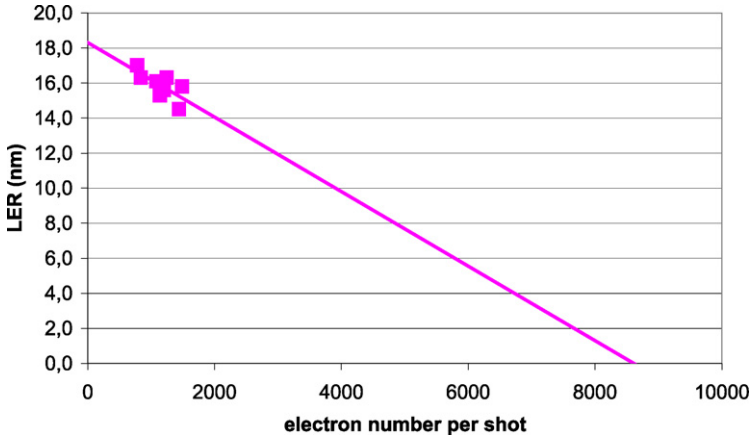


Fig. 10. LER evolution versus electron number per shot for patterning a 70 nm dense structure.

the substrate. Back-scattered electrons are thus generated, depositing additional energy on a wide area around the beam. The depth and the radius of the back scattered electrons depend on the initial beam energy and the substrate composition. The modeling of forward and back scattered electrons by Monte-Carlo calculation helps to determine the energy distribution through the resist (Fig. 11).

So, based on this simulation approach, proximity effects can be compensated by tuning locally the exposure dose. Several solutions exist on the market to provide the dose correction to be applied [16,17]. Some are linked to the hardware of the machine itself and exposure dose is set on the fly. Others solution are software-based, like PROXECCO, developed by PDF Solution. Using shaped beam system the limitations of CD control proposed by the dose modulation principle have been already highlighted [18]. Fig. 12 presents an example of the linearity control of an isolated feature. The graph shows that, for a qualified resist model, dose modulation solution provides a good CD linearity control down to 70 nm and is no longer efficient below. This CD linearity can be fine tuned by optimizing the beam interactions with the introduction of complex model with 3 to 5 Gaussian approximations. However this type of approach significantly increases fracturing steps and is metrology time consuming for model building.

However, whatever the dose model tuning, there is always one process aspect that is not properly corrected. Effectively, the requested accuracy to resolve sub-70 nm feature size is one concern for process development, but the control of the line end, corner rounding is a key parameter too for final product functionality. Fig. 13(b) presents an example of 45 nm CD active level with only dose modulation correction for proximity effect correction. An important shortening of the line end can be observed after lithographic processes versus the original design (Fig. 13(a)). To overcome this

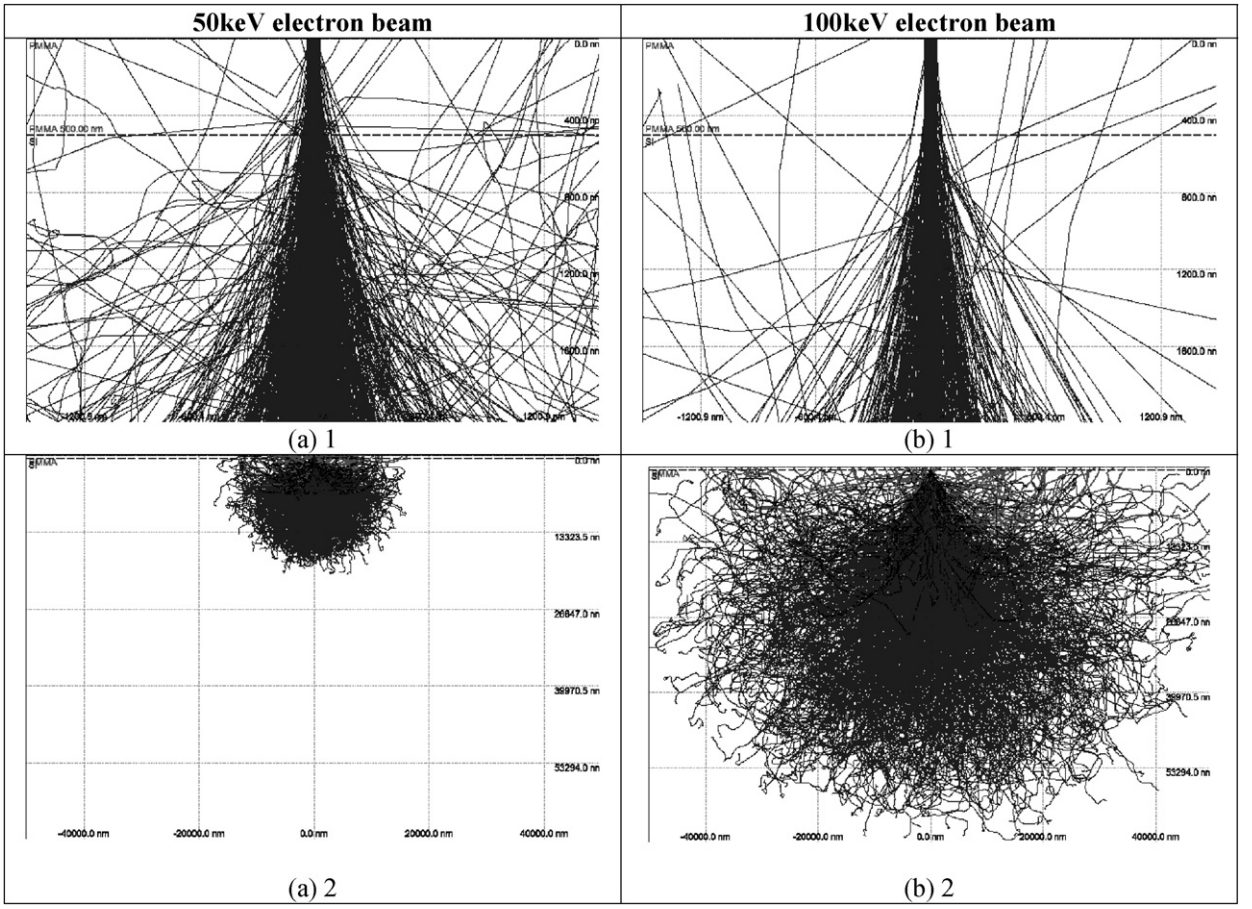


Fig. 11. Monte Carlo simulation of forward and back scattered electrons within 500 nm thick PMMA on silicon substrate (a) with 50 keV, (b) with 100 keV electrons. Top views show the forward electron trajectories and the potential CD gain, increasing e-beam energy. The lower views show the forward electron and the back electrons trajectories, which are as much more scattered as the energy increases.

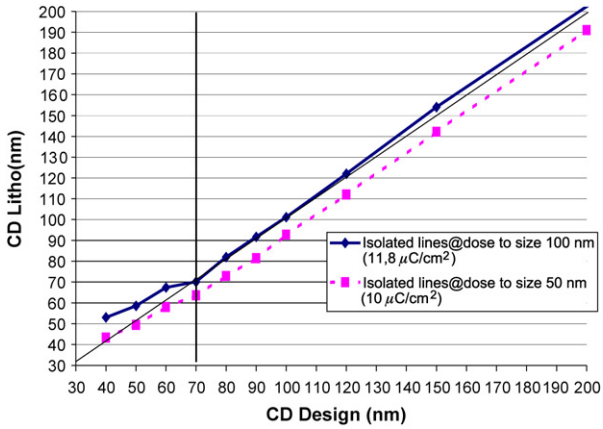


Fig. 12. Linearity control with dose modulation control only.

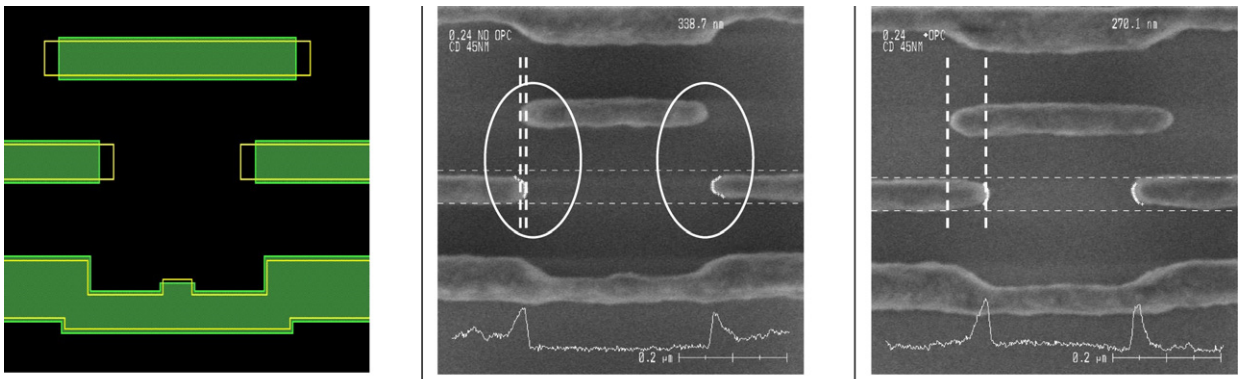


Fig. 13. Line end shortening for 65 nm half pitch node with e-beam ruled based correction, active layer definition.

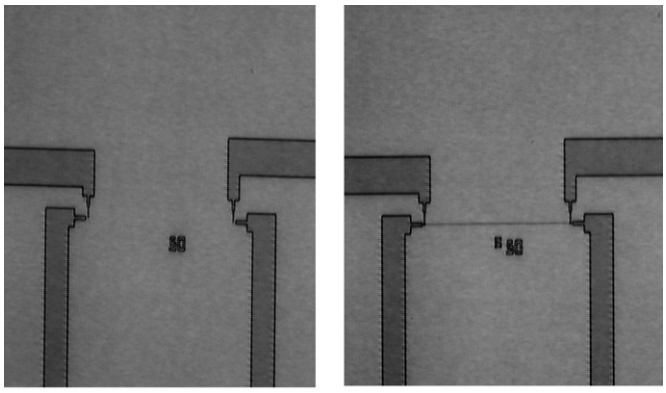
issue, the insertion of basic geometrical correction becomes mandatory to ensure the final pattern fidelity. Fig. 13(c) highlights the quality improvement of the active lithography after the implementation of this complementary solution.

The mixed solution with dose and geometrical corrections seems to be mandatory today for the patterning of sub-70 nm feature size by using shaped beam systems. This concern is not yet so critical for e-beam mask maker, as patterns are $\times 4$ larger than on a wafer for the same technology. However, with the introduction of sub-resolution assist feature, special attention will be necessary for the realization of sub-45 nm node masks. Finally, the generalization of a geometrical correction in addition to dose control for direct write lithography, represents an efficient solution mandatory to extend an accurate CD control.

4. The golden solution for advanced R&D purpose: the Gaussian beam alternative

Gaussian beam lithography has been the work force for advanced research and development in a wide range of applications. This technology has been used primarily for its high resolution capability and its flexibility. CMOS scaling was possible, well in advance of optical lithography tool introduction at the desired node, allowing the development of new architectures and new materials [19].

The achieved resolution, in the range of few nanometers, allows investigating alternative devices to CMOS technology, such as: Single Electron Transistor (SET), quantum devices, spintronics and molecular electronics. The flexibility of e-beam lithography has also been widely used for a large variety of studies, such as: DFB laser, photonic crystals, surface acoustic waves devices, 3D structuring...



(a) DUV exposure only (b) DUV and e-beam exposures

Fig. 14. Hybrid lithography principle.

Even if in the field of advanced research the primary concern is resolution, throughput is still an issue for a Gaussian beam. To overcome this problem, a new writing strategy has been proposed: hybrid lithography [20]. Due to resist process compatibility, hybrid lithography, which is based on the sequential exposures of optical and e-beam lithography on the same resist, allows us to reach the highest resolution with e-beam and the necessary throughput with the optical stepper. With the introduction of DUV lithography, a new generation of CARs has been developed. This family of resist is totally compatible with e-beam lithography allowing the patterning of the same resist with both an e-beam tool and a DUV stepper (hybrid lithography). A standard optical DUV resist is coated then e-beam exposed for high resolution patterns and DUV for larger dimension patterns then simultaneously developed, as shown in Fig. 14.

5. The shaped beam: a first alternative for semiconductor manufacturing

The shaped electron beam systems are today mainly used for advanced mask realization. They replaced the standard optical systems for advanced mask realization. The high resolution provided by e-beam associated to the throughput opportunity represented by the shape projection principle and a better image placement mainly explained the EBDW insertion. However, the direct write concept for manufacturing application was still marginal due to the low throughput of the e-beam systems. However, with the optical manufacturing cost trend presented in Section 2.3, the interest of this technique for low volume application starts to offer promising cost and cycle time gain opportunities. First, shaped beam tools can be employed for advanced R&D [21]. It allows starting the development of the future generation of the integrated circuits (IC) by printing all critical levels well in advance of the current resolution capability of the optical scanners. Then, thanks to a good reactivity and flexibility, they can be used for new product manufacturing start ahead of mask realization, product customization for anti-piracy and flexible programmable markets [22].

Based on the full integration capability of e-beam processes detailed in Section 3, examples of the demonstrations which have been performed in the last years within the Crolles2 Alliance programs where 2 VISTEC SB350DW are operational. On Figs. 15 and 16 some realizations are presented [23,24].

However, for a real interest for low volume manufacturing addressing the prototyping market, the throughput issue has to be addressed. With the average of one wafer per day for a 90 nm half pitch product, the manufacturing reactivity needs totally to be improved. The insertion of the Cell Projection concept (CP) is an alternative to push shaped beam platform capability [25]. The insertion of a stencil containing library elements offers shot reduction opportunities. Japanese companies, like HITACHI, ADVANTEST and more recently E-BEAM Corp., propose such an alternative. Depending on product design and application, shot number reduction can reach 70% versus a standard single beam system, as presented in Fig. 17. Including all the tool improvements that can be introduced with a new platform system in terms of overhead, stage speed for example, the potential of a shaped beam system with CP option could push throughput down to 1 wafer per hour. At this level of writing speed, EBDW system becomes a real and credible solution for prototyping.

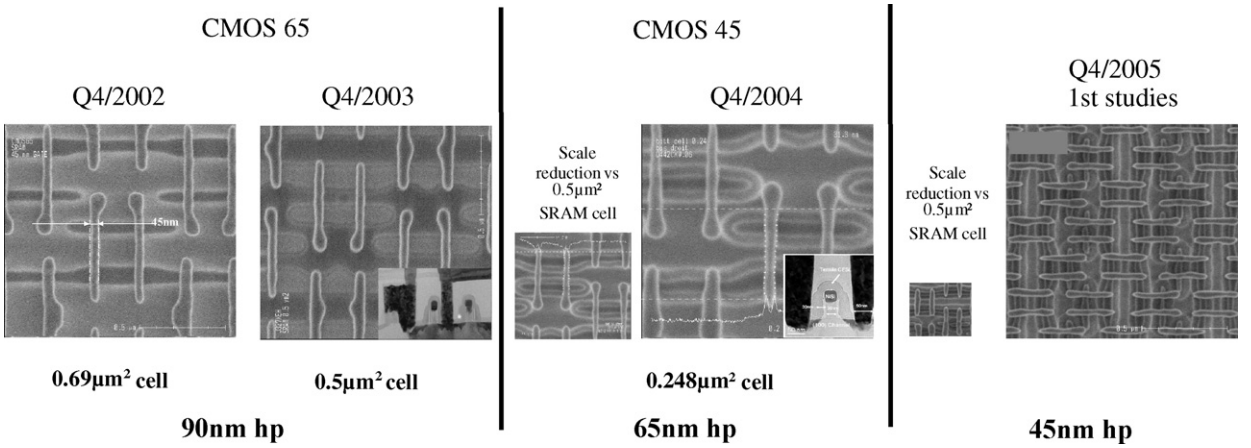


Fig. 15. Examples of advanced circuits developed at Crolles2 on EBDW platform from 2002 to 2005.

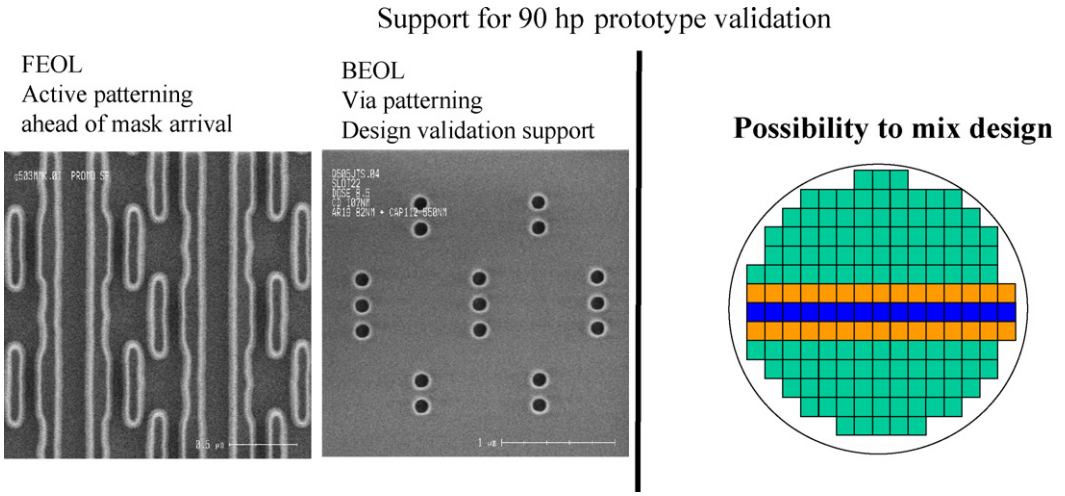


Fig. 16. Low volume support activity for manufacturing reactivity and flexibility.

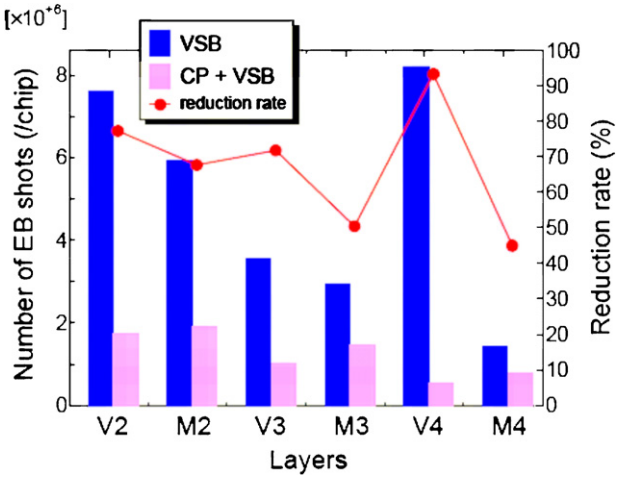


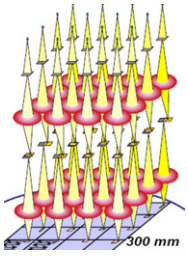
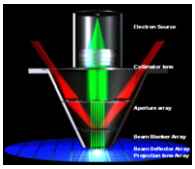
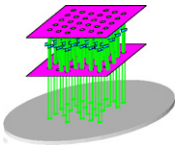
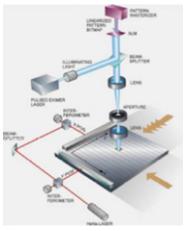
Fig. 17. Shot reduction opportunity with CP concept introduction [26].

6. The multi-beam perspective

The single beam technology does not meet the manufacturing requirements in term of throughput. Fast direct write projects are under development to fulfill this requirement and to address the low volume production market. Several approaches are under development (Table 2):

- *Single shaped beam with massive CP concept*: this project is supported by E-BEAM Corporation. The concept is to identify a common cell library for an entire technology node. Then, a stencil is generated that will allow printing in one flash all these repetitive structures. The stencil can accommodate as many as 400 different cells. Proximity effects are limited due to the low accelerating voltage. A gain in throughput of around 4 to 5 wph@65 hp is foreseen with this solution [27].
- *Multi-column strategy*: ADVANTEST is working on this concept. It consists of building an array of independent 50 kV single beam columns with up to 16 units with 100 CP characters each. Each column writes a specific part of the wafer which limits stage displacement overheads. The throughput with this platform is targeted to reach between 5 and 10 wph@65 hp, depending of the CP library optimization [28].
- Multi-beam with charged particle: the concept is to generate multi-beam from a flood exposure through an aperture plate array. The initial beam is split in thousands of elementary beams. Each beam is switched on and off and deflected independently. Two projects are presently identified:
  - The first, proposed by MAPPER, is based on low accelerating voltage to reduce proximity effect concerns. For this project, data are sent to the system through an optical link controlling the switch of the beam. This allows a very fast data rate exchange, 7.5 GHz per beam. The future platform targets aggressive throughput of 10 to 30 wph@45 hp [29].
  - VISTEC is also proposing a similar multi-beam concept using high accelerating voltage at 100 kV. In this case, the beam is blanked by an electrostatic field. Throughput expectations are in the range of 5 wph@45 hp [30].
- *Multi-beam with photon*: In optical Maskless Lithography (OML) the illumination light is reflected from a dynamic pattern generating device called Spatial Light Modulator (SLM). The SLM is made of an array of tilting

Table 2
Fast throughput system ML2 platform overview

Company name	EBEAM Corp.	ADVANTEST	MAPPER	VISTEC	ASML
Principle	VSB + CP 400 characters	Multi columns with shape beam & CP concept 100 characters	Multi-beam	Multi-beam	Multi-array
Source	Electron	Electron	Electron	Electron	Photon
Accelerating voltage	5 kV	50 kV	5 kV	100 kV	NA
Demagnification number				400	400
Beam number	1	16 columns	13 000	10 000	100 Mpixel 26 × 32 mm
Spot size	VSB spot	VSB spot	35 nm	25 nm	40 nm
Throughput (wph)	1–5	1–10	10–30	5	5
Technology node insertion	65 hp	65 hp	45 hp	45 hp	65 hp
					

micromirrors which will form a grey scale image then the pattern is imaged onto a substrate through a high de-magnification projection lens. The know-how from optical lithography is directly applicable to this solution (source, optical, resist, immersion principle). ASML proposes an optical mask less for the 65 nm half pitch technology with a throughput target of 5 wph [31].

- *Multi-source concept*: another source concept is presently under development. The elementary beam is composed by a field emitter array amplified by micro channel amplifier. The advantage of this approach is its high brightness provided by the multi-source approach. The proposed solution is also scalable to thousands of beam offering throughput increase capability. The American companies ARRADIANCE and MBS develop today a first source demonstrator that could be potentially integrated in a near future by a tool manufacturer [32].

As presented in this previous description, a lot of ML2 projects exist on the paper. With an average throughput between 5 to 30 wph, each system offers a real opportunity for the low volume market, whose interest is specially enhanced with lithography cost forecast. However, the first concern of these future systems is the introduction point into manufacturing. In 2009, 65 nm half pitch should be qualified for manufacturing while 45 nm node should be under qualification. Consequently, a tool with only 65 nm half pitch specification seems to be introduced too late for manufacturing, as main stream optical processes will be already qualified. On the contrary, provided their availability by the end of this decade, systems with 45 nm half pitch capabilities appear to better placed.

Difficulties for ML2 insertion is that no company has today announced officially its intention to start manufacturing tool development. The main reason is the low maturity development of all these projects. In addition, as ML2 technology interest is mainly dedicated for ASIC manufacturing representing 10–20% of the lithography tool market, financial support for these projects is lower compared to the 'main stream' lithography projects like high index immersion or EUV. Nevertheless, most of the ML2 companies are pursuing their efforts and developing presently first demo concept systems available between mid 2006 and mid 2007 to validate source and data transfer aspect. Then, first beta systems could be foreseen between 2009 and 2010. But, before integrating this technology into manufacturing, a lot of open issues will have to be evaluated and qualified. Among them, we can underline data fracturing and proximity corrections where low level development is today performed. However, it is sure that the first manufacturer providing a commercial system that will be integrated into manufacturing will capture this market and acquire a leading position on ML2.

7. Conclusions

Electron beam lithography is a well known and mature technology which has been used for decades in the research and development environment giving both high resolution and flexibility. Due to the rising cost of optical lithography, both for tools and masks, EBDW has regained attention and is foreseen as a viable alternative for low to medium volume production.

Issues such as alignment strategy, resist technology, proximity effect corrections have been addressed in a production environment and have found satisfactory solutions. Nevertheless, throughput is still the main issue for EBDW and new systems based on multi-beams or multi-columns concepts need to be put in place for addressing high volume production.

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