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Ultimate lithography/Lithographie ultime

# An introduction to ultimate lithography

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**Abstract**

Lithography has been the key enabler for scaling feature sizes of integrated circuits, allowing the exponential growth of the semiconductor industry. This article will briefly describe the major challenges of this technology in microelectronics and introduce the review articles presented in this special issue. ***To cite this article: M. Brillouët, C. R. Physique 7 (2006).***


**Résumé**

**Une introduction à la lithographie ultime.** La lithographie a été le facteur clé pour réduire les tailles de motifs des circuits intégrés, ce qui a permis une croissance exponentielle de l'industrie du semiconducteur. Cet article décrira brièvement les enjeux majeurs de cette technologie en microélectronique et introduira les revues présentées dans ce dossier. ***Pour citer cet article : M. Brillouët, C. R. Physique 7 (2006).***


Lithography is a technology allowing printing extremely small and complex patterns on a silicon wafer. By scaling feature sizes of integrated circuits (ICs) down to few tens of nanometers, the lithographic technique has been and is a key factor in realizing Moore's law, i.e. putting more and more transistors in a single IC and consequently allowing the exponential growth of the semiconductor industry.

Lithography is also central in another respect. Manufacturing ICs on a silicon wafer consists of repeating many similar process sequences (see Fig. 1). Typically a material is deposited on the wafer. A photosensitive polymer (the 'photoresist') is spin coated on the wafer and the image of a mask pattern is projected onto this layer. After some specific process steps involving photochemical reactions in the resist, the exposed areas of the photoresist are dissolved. The uncovered substrate can then be locally etched where the resist is removed. Alternatively impurities can be driven into the substrate at the location of the resist openings. The remaining resist is subsequently stripped and another cycle of deposition-lithographic sequence can be restarted. Advanced technologies need to print more than 30 different patterns in the different deposited layers of a silicon wafer, which means that lithography is one of the most intensively used process in silicon IC technology.

The ultimate resolution $R$ obtained by this lithographic process is given by:

$$R = k_1.\lambda/\mathrm{NA}$$

where $\lambda$ is the exposure wavelength, NA the numerical aperture of the projection optics and $k_1$ is a technology-related factor. Each of these factors corresponds to a specific way to improve the resolving power of the lithography:

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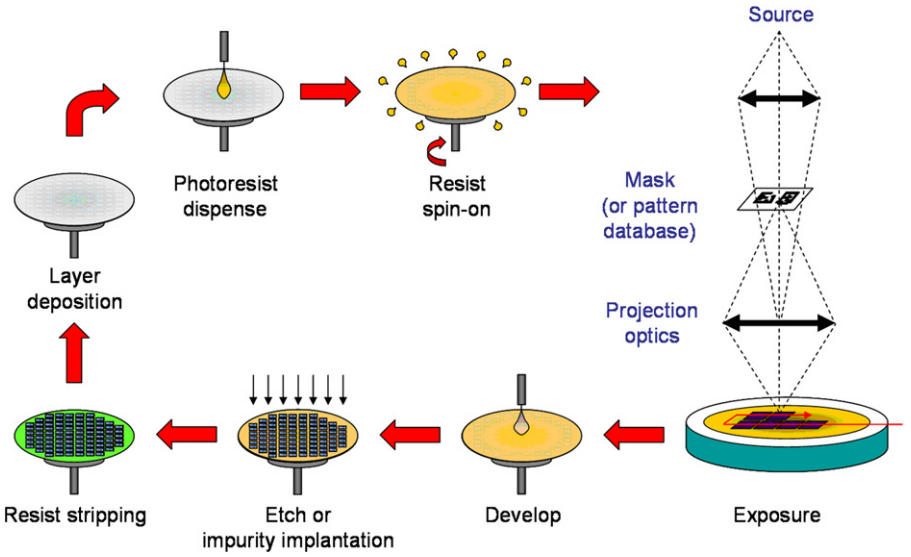


Fig. 1. Simplified sketch of a process flow for manufacturing integrated circuits, showing the central role of the lithography.

- Decreasing λ was a general trend in the history of the microelectronics industry:
  - In the 1980s the first tools used a mercury arc lamp (λ = 436 nm—g-line, 405 nm—h-line or 365 nm—i-line) and most often a de-magnifying refractive projection optics made of quartz;
  - The industry moved in the late 1990s towards lower wavelengths using a deep UV laser illumination (248 nm—KrF laser and then 193 nm—ArF laser), achieving a half-pitch resolution below 90 nm;
  - The next wavelength change was expected to be using a $F_2$ laser (λ = 157 nm), but the introduction was delayed sine die due to major technical challenges;
  - The next generation lithography is expected to use EUV radiation (λ = 13.5 nm). This is a major step forward in that, due to the strong absorption of any material at this wavelength, reflective optics should be used along with specific resist processes. Many technical and economical issues have still to be solved before this future lithography being introduced in a fabrication line.

  It should, however, be noted that changing the wavelength results in the necessity for extensive efforts, as the resist material and process have to be studied for each new wavelength along with the associated etching process. Moreover, the lithographic tool may need a new architecture and possibly new materials (e.g. $CaF_2$).

- Increasing NA is the preferred approach while staying with a given λ. The development of the exposure tool involves few disruptive concepts and the state-of-the-art manufacturing tools provide a NA in the 0.9 range. A recent breakthrough was obtained using immersion lithography (in that case, a liquid layer with a higher refractive index is interposed between the lens and the photoresist) through which a NA higher than 1.0 can be obtained. This could give a further life to the 193 nm lithography before moving to EUV.
- Lowering $k_1$ (the so-called 'Resolution Enhancement Techniques' or RET) is a technique research teams worked on from the early 1990s and where impressive results have been obtained. More specifically, progress has been made:
  - by tuning the resist process (higher contrast, control of the diffusion of the photo-active species, etc.);
  - by adjusting the illumination (annular, quadrupole, etc.). In some cases, however, this technique leads to results which are depending on the pattern;
  - by tuning the phase of the exposure light, using Phase Shift Masks, in order to increase the contrast of the resulting image;
  - by adding or modifying specific features on the mask whose contribution will 'correct' the resulting aerial image at the wafer surface and in many cases improve the resolution or process latitude: this technique is widely known as OPC or Optical Proximity Correction. The major drawback of this approach is that the mask man-

ufacturing becomes extremely demanding: more features are added, resulting in an exponentially increasing cost and the introduction of phase-shifting pattern makes the control and repair of the mask more complex.

As the mask industry is facing major economical challenges, it brings a renewed interest in maskless technologies, especially using electron beams (or e-beams). Although this approach is not new and may be of wide use for advanced laboratory-type experiments, e-beam lithography did not show up as a mainstream technology in volume manufacturing owing to the low throughput of the equipment. However, promising perspectives are explored giving some hope that it could be a contender of EUV lithography for some industrial applications at the 32 nm half pitch technology and below.

It is comfortable to think that as soon as the targeted resolution is obtained, one is able to obtain a high integration density of functions on an IC. This is unfortunately not true. An IC is a stack of different layers and patterns which should aligned with respect to each other. It does mean that the accurate overlay of a pattern on another one is a key contributor to the final integration density. Depth of focus (DoF) is another concern, putting more emphasis on the resist process: this is especially true with the higher numerical aperture of advanced tools, as the DoF is expected to be inversely proportional to the square of NA. It should finally be stressed that metrology—and, more generally speaking, process control—becomes more challenging as we are entering the nanometer regime.

In summary, lithography is a central technology in the semiconductor industry achieving breakthroughs by revisiting often well-known optics and chemical concepts and using then in an innovative manner. This Special Issue of the *Comptes rendus Physique* dedicated to the Ultimate Lithography will bring an in-depth discussion of all these challenges.

In an introductory paper K. Ronse of IMEC – Belgium will take a look on optical lithography from an historical perspective. This article will describe the breakthroughs which allowed photolithography to fulfil all the requirements of advanced volume manufacturing despite pessimistic predictions that optical lithography will run out of steam very soon. Summarizing the few principles of optics which drive the progress in optical lithography, he will describe the significant evolutions in the exposure tool and in the photoresist, in reducing the exposure wavelength and more recently by taking advantage of the light coherence and correcting proximity effects. Finally, he will also address some recent trends in photolithography.

In a subsequent paper B. Lin of TSMC – Taiwan will discuss the limits of dry lithography systems and the exciting perspectives offered by the immersion lithography, pushing the optical technology to its very limit. Many aspects of this emerging approach will be treated, including defects, polarized illumination, high-index materials, solid-immersion mask, double exposure and double patterning.

The challenges of EUV lithography will be addressed by K. Kemp and S. Wurm in their assignment at Sematech – USA. Extreme ultraviolet lithography (EUVL) technology and infrastructure has made excellent progress over the past several years, and tool suppliers are delivering alpha tools to customers. However, requirements in source output power, mask defect reduction, optics quality, and resist (including resolution, line width roughness, and photospeed) are very challenging, and significant development efforts are still needed to support beta and production-level performance. We should not also forget the economical factors, especially cost of ownership and extendibility to future technology generations which may determine the outlook for the manufacturing insertion of EUVL. If the technical and business challenges can be met, then EUVL will be the likely technology of choice for semiconductor manufacturing at the 32 nm half-pitch processes and beyond.

Starting from the 120 nm CMOS technology node, we have entered into a new lithographic regime, the so-called ‘sub-wavelength imaging’, moving closer to the theoretical optical resolution limit and implying bigger image distortion between the mask and the final result on silicon. Resolution Enhancement Techniques (RET) have been developed in order to print all shapes properly. This will be discussed in the fourth article by Y. Trouiller from CEA–LETI – France. As a part of the RET approach, OPC (Optical Proximity Correction) has been widely used by doing mask pre-compensation of all non linear effects, optical diffraction and interference effects, resist and etch. From its first industrial utilization for 120 nm node to 32 nm prospectively, many evolutions have been seen for OPC with some specialization for different types of products (e.g. memories or logic devices). These include generalisation to all lithographic layers, moving to pixel based simulation, usage of full chip simulation verification, the incorporation of process window effects like energy latitude or depth of focus into the OPC algorithm, and inverse lithography approach.

These advanced image correction techniques put more burdens on the mask industry. In his article, C. Reita (formerly from Photronics and now with CEA–LETI – France) will briefly outline the fabrication of masks and discuss in more details some specific aspects, especially the new issues related to the manufacturing and control of such advanced masks along with the economical impacts that may affect the whole IC supply chain.

The increased cost of a state-of-the-art mask set which may strongly exceed the million of US dollars raised a renewed interest in maskless lithography (ML2) and especially in electron beam based systems which are the most mature maskless technology. If the present use of e-beam lithography in small scale manufacturing can be extended through high throughput machines to the 32 nm half-pitch high volume technology, it would become a serious competitor to the EUV lithography. In their paper Laurent Pain, Serge Tedesco and Christophe Constancias of CEA–LETI – France will present the different technological solutions and the associated process challenges in present and future ML2 approaches.

Any lithographic technique relies on some kind of sacrificial imaging layers: photosensitive polymers were steadily improved to keep up with the innovations in the lithography tools. It is noteworthy that changes in exposure wavelength and more recently the advent of immersion lithography put more pressure to understand and better control the photochemistry of these materials in the quest for higher fidelity in the pattern transfer. The article of B. Mortini of STMicroelectronics – France will shed some light on the difficult issues photoresists are facing today.

In a recent past, optical microscopy and later SEM-based measurements were sufficient to assess the dimensional results of a lithographic operation. More recently scatterometry was developed to give some insights in the shape of a periodic pattern. However controlling the shape and size of the pattern on silicon becomes more and more challenging as we are considering nm-sized features. S. Knight and coworkers of NIST – USA will discuss the current state of the art in the metrology for measuring critical dimensions of printed features using scanning electron microscopy and atomic force microscopy, and how the National Institute of Standards and Technology helps advancing these tools. Exploratory work on two new promising techniques, scatterfield microscopy and small angle X-ray scattering, will be then detailed.

As in any technical domain experts use a jargon which may be difficult to understand for the non-specialist. To help the reader, we added a glossary of terms which may be not self-explanatory in the articles of this Special Issue on Ultimate Lithography.