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Ultimate lithography/Lithographie ultime

Glossary

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248, 193 nm Wavelength of excimer lasers (KrF and ArF, respectively) used in the most advanced lithography tools.

0.93 NA Numerical aperture of the projection optics whose value is given by the number preceding NA (in this case 0.93). Maximum NA value in air is 1.0.

32 hp or *32 nm hp* 32 nm half-pitch (*see* Half-pitch).

0.35 k_1 A lithography whose k_1 value is 0.35. k_1 is a proportionality factor in the formula:

$$R = k_1.(\lambda/\mathrm{NA})$$

giving the achievable resolution R of a lithography technique for a given exposure wavelength λ and numerical aperture NA.

1x, 2x Magnification ratio of the lithography tool. Optical lithography tools (scanners) are using today a 4x magnification.

α-tool First fully integrated tool allowing assessing the major improvements needed for a manufacturing-worthy tool.

ARC AntiReflective Coating. A layer deposited above or below the photoresist in order to minimize reflections during the exposure by producing destructive interference in the reflected beam and/or by absorbing the unwanted reflection. This layer can be either organic or inorganic (in the later case it is usually a SiON dielectric) and it is deposited either above (Top ARC or TARC) or below (Bottom ARC or BARC) the resist layer.

ArF 193 nm lithography using an ArF laser.

ASIC Application Specific Integrated Circuit. An ASIC is an integrated circuit designed for a particular use. For the lithographer it does translate as a circuit layout whose pattern is complex and not very regular (often characterized as 'random'). For the manufacturer it means a product with limited volume and tight time to market.

β-tool Fully integrated tool which permit the full assessment of the technology in a manufacturing environment.

Bake Thermal annealing of the photoresist.

BARC *see* ARC.

BIM Binary mask. Standard mask using an absorbing layer structured in a printable pattern. This layer totally blocks the light and the binary mask does not use a phase-shifting or partially absorbing layer.

CD Critical Dimension. Width of a pattern or of the distance between two patterns.

Cost of Ownership Cost estimate designed to help managers assessing the total cost of an investment, including the acquisition, the installation, the running cost and potentially the decommissioning. The running cost includes all the operational cost, including consumables, preventive and corrective maintenance, non-productive overhead, etc.

Die Piece of silicon containing the complete integrated circuit to be manufactured and being packaged after dicing. It should be distinguished from the projected image of a reticle in a stepper (*see* definitions below), which may contain many different dies.
Also called *chip*.

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DoF Depth of Focus (or Depth of Field). Latitude in the position of the imaging plane (i.e. of the image in the photoresist on a wafer) where the specified resolution and pattern quality can be achieved in the photoresist. It is usually referred as a plus or minus deviation from a reference plane.

DUV Deep Ultra-Violet. Usually understood as a wavelength below 300 nm, it translates for optical lithography as 248, 193 and 157 nm wavelengths corresponding to KrF, ArF and F_2 excimer lasers.

Exposure latitude Range of light intensity (or other lithographic irradiating energy) where the specified resolution and pattern quality can be achieved in the photoresist.

EUV Extreme Ultra-Violet. Very energetic light (though usually more than 30 nm). In the context of the EUV lithography, it is related to a light source whose wavelength is 13.5 nm (which strictly speaking should have been named soft X-ray).

Flare Unwanted light scattered in the lens system, such as internal reflections and scattering from material inhomogeneities, or from the edges of pattern of the mask.

Foundry IC manufacturer who produces devices from different customers on demand but does not design the product. It is usually opposed to IDMs (Integrated Device Manufacturers) who design, manufacture and sell products.

Full field (tool) As opposed to a micro-exposure tool a full field lithographic tool is able to print a full reticle field (typ. more than 2 cm a side) in a single step or scan on a wafer.

Half-pitch Estimate of the maximum pattern density on a circuit for a given technology. The actual value of the most aggressive half-pitch is no more a single target value for the whole microelectronic industry, but depends on product type. For ASIC, microprocessors and dynamic memories (DRAMs) it represents half the pitch of the contacted first metal level. For non-volatile memories (flash) it indicates half the pitch of the uncontacted polysilicon level.

Hardbake Thermal annealing of the resist after development in order to harden it for subsequent processes (e.g. dry etch or ion implantation).

i-line Hg line at 365 nm. This wavelength is used for less advanced technologies.

IC Integrated Circuit.

IDM *see* Foundry.

k_1 *see* 0.35 k_1.

Killer defect A defect on the mask or on the wafer which will produce a non-functional integrated circuit. The 'killing' efficiency of a defect depends on its size (for a given technology) and its location. If this defect is on the mask used for a stepper or scanner, it will be duplicated on all dies reducing the final yield to zero.

KrF 248 nm lithography using a KrF laser.

Layer On a wafer it represents any kind of uniformly deposited material.
In lithography it is the pattern to be printed at a given stage of IC manufacturing (in the most advanced technologies the full fabrication flow of an integrated circuit amounts to more than 30 layers).
In the mask industry it can be a subset of the design data to be assembled on the final mask or reticle.

Level In lithography often synonymous with 'layer'.

LER Line Edge Roughness.

Linewidth Lateral dimension of a pattern. It is measured as the distance between two edges of the material pattern at some specified height above the interface with the substrate.

LWR Line Width Roughness.

Manhattan design Most of pattern (esp. interconnects) in an integrated circuit are laid out along the x and y directions: the so-called Manhattan design or architecture refers to this feature which takes the analogy with the way streets are organized in Manhattan's borough of New York City.

Mask Plate which comprises patterns to be imaged in a photoresist through a lithographic tool. The mask is usually transparent as in the optical lithography where it is used in a transmissive mode, or reflective as in EUV lithography.

MEF Mask Error Factor. This concept was developed as the printed feature became much shorter than the exposure wavelength leading to nonlinear imaging. The Mask Error Factor is defined as the ratio of the change in CD on the printed wafer to the CD change on the mask after reduction. A mask error factor of 2.0 means that, a 10 nm CD error on a mask after reduction (a 40 nm error on a 4x reticle) will result in a 20 nm CD error on the wafer rather than the 10 nm error that would result with linear imaging and a MEF = 1.0.

Micro(field) Exposure Tool or *MET* Small scale lithographic tool allowing the projection of a pattern whose size on the wafer is typically less than 1 mm a side. This equipment is used for an early assessment of a new lithography technique before the availability of a full-field tool.

Node (technology node) In the earlier International Technology Roadmaps for Semiconductor, technology generations were described as technology nodes expressed as a dimensional measure (e.g. 45 nm node). From 2005 owing to the different critical dimensions related to different products (e.g. logic, DRAM or flash) this concept was replaced by a definition of the half pitch (*see* Half-pitch).

Overlay The precision with which successive images can be aligned with respect to previous patterns on a silicon wafer.

PAC PhotoActive Compound, i.e. the chemical compound in the photoresist which is responsible for its imaging capability.

PEB Post Exposure Bake. Thermal treatment of the resist after exposition and before development. It helps to diffuse the photoactive compound minimizing standing wave patterns. More recently for chemically amplified resists the catalytic deprotection by the photo-generated acid is obtained through this bake.

PSL PolyStyrene Latex spheres. These spheres which can be made monodisperse are used as dimensional standards for particulate contamination measurements.

PSM Phase Shift Mask or Phase Shifting Mask. Mask that shifts the phase of the light to improve the imaging performance of the lithography.

Resolution Minimum achievable size of a pattern on a wafer.

Reticle Mask used in a stepper or a scanner.

Scanner Step and repeat lithographic tool (*see* 'Stepper' below) in which an illuminating slit is scanned over the mask for projection onto the wafer. It helps to limit the optical distortions for a given field size.

Softbake Thermal treatment of the resist before exposure in order to drive out solvents and densify the resist.

Stepper Step and Repeat tool. Lithographic tool where the mask pattern is imaged in a small area of the resist-coated wafer and the imaging process is repeated on many different locations of the wafer by small steps in the X and Y directions.

Straylight *see* Flare.

TARC *see* ARC.

Throughput Number of wafers a machine can run per hour, assuming 100% tool uptime and no waiting/queuing time.

Via Opening (or hole) in the intermetal insulating layer of an integrated circuit through which a conductive path can be made between two metal lines at different levels.