C. R. Physique 11 (2010) 381–388

Contents lists available at ScienceDirect

Comptes Rendus Physique

www.sciencedirect.com

Optical properties of nanotubes / Propriétés optiques des nanotubes

CNT integration on different materials suitable for VLSI interconnects

Intégration de nanotubes de carbone sur différents matériaux représentatifs des connexions dans les circuits intégrés

Hanako Okuno [a,*], Adeline Fournier [a], Etienne Quesnel [a], Viviane Muffato [a], Helene Le Poche [a], Murielle Fayolle [b], Jean Dijon [a]

[a] *CEA, LITEN/DTNM, 17, rue des Martyrs, 38054 Grenoble cedex 9, France*
[b] *CEA, LETI, 17, rue des Martyrs, 38054 Grenoble cedex 9, France*

ARTICLE INFO

Article history:
Available online 11 August 2010

Keywords:
Carbon nanotubes
Via interconnects
Integration
CVD

Mots-clés :
Nanotubes de carbone
Structures vias
Intégration
CVD

ABSTRACT

We have succeeded in direct integration of carbon nanotubes (CNTs) for via interconnects using different back contact materials. Highly doped Si and poly Si are used, aiming at the CNT via interconnects directly from source, drain and gate of transistors. In addition, we propose to use aluminum copper alloy (AlCu) as a metal line because of its higher conductivity compared that of copper in very small geometries. The experimental conditions for CNT growth are optimized on these three substrate materials, which are applied for the direct integration in via holes with success. The achieved density in 1 µm via holes is more than 10^{12} cm^{-2}, the highest value reported so far.

RÉSUMÉ

Nous présentons l'intégration de nanotubes de carbones (NTC) dans des structures vias submicroniques comportant différents matériaux de contacts inferieurs. Ces matériaux silicium dopé et poly silicium sont représentatifs des connexions sur les électrodes (source drain grille) des transistors. Pour les connections sur métaux dans la partie « *backend* » du circuit intégré, nous proposons d'utiliser un alliage l'aluminium cuivre (AlCu) qui présente une meilleure conductivité que le cuivre pour des lignes de petites dimensions. Les conditions expérimentales pour la croissance de NTC ont été optimisées sur chacun de ces substrats. La densité de NTC atteinte dans des via d'un µm de diamètre est supérieure à 10^{12} cm^{-2}, ce qui est la valeur la plus importante publiée à ce jour.

1. Introduction

Interconnects, because they constitute up to 70% of the total on-chip capacitance [1], are representing a major bottleneck for giga- and tera-scale electronic systems because of the RC delays they add, the power dissipation, the cross-talk dissipation and the vulnerability to electromigration. Furthermore, resistivity is a growing concern as the line width scales down in order to meet the International Technology Roadmap for Semiconductors (ITRS) requirements of actual and upcoming

* Corresponding author.
E-mail address: hanako.okuno@cea.fr (H. Okuno).

1631-0705/$ – see front matter
doi:10.1016/j.crhy.2010.06.008

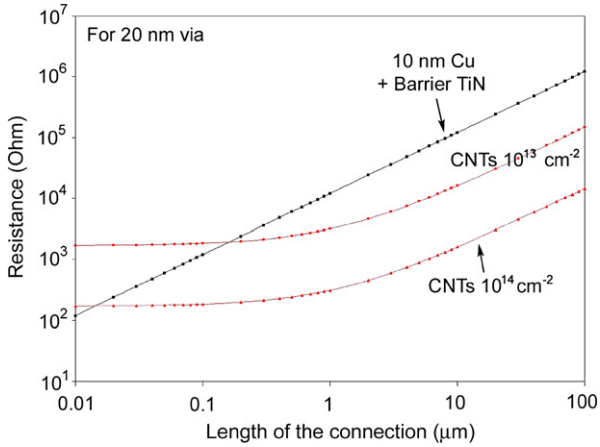

Fig. 1. Low-field resistance of Cu and ultimate SWCNTs interconnects compared as a function of their length.

technological nodes: the actual feature size is approaching the mean free path of electrons in Cu (40 nm, [2]) which causes a rising of current density and increasing of Cu resistivity. It is thus necessary to investigate new materials to overcome such physical limitations and therefore allowing the extension of Moore's Law. Carbon nanotubes (CNTs) might be also a valid alternative to Cu for VLSI interconnect applications due to their outstanding electrical and thermal properties. CNTs can carry three orders of magnitude larger current densities than Cu without showing signs of electromigration failure; in particular metallic CNT represents a promising material to replace Cu as an interconnect material mainly because they have unusually large mean free paths (in the μm range, [3]) and unmatched electromigration resistance. The quantum resistance of a CNT is $R_Q = 6.5\ \mathrm{k}\Omega$ [4,5], which is independent of the CNT diameter up to 20 nm [6]. This is a big technological advantage as a precise diameter control of the CNTs might not be needed for the application. In order to compete with Cu, a large number of conduction channels have thus to be positioned in parallel, which means that high density CNT materials have to be developed and integrated in devices in order to make a realistic connection. Finally, as opposed to the case of metals, the thermal conductivity of CNT increases when temperature increases, heat dissipation is one of the major challenges of the shrinking of device dimension in VLSI. The density of a hexagonal compact array of tubes with a diameter d_{CNT} is given by

$$\rho = \frac{2}{(d_{CNT} + e)^2\sqrt{3}}$$

where e is the distance between two carbon walls (0.34 nm) assuming that in a CNT bundle the minimum distance between tubes is e [7]. This indicates that the maximum tube density we can achieve with 3 nm diameter CNTs is $10^{13}\ \mathrm{cm}^{-2}$. In the case of DW or TWCNTs, a conduction wall density of $10^{13}\ \mathrm{cm}^{-2}$ is achievable with 4 nm diameter tubes. The theoretically calculated ultimate density is close to $2 \times 10^{14}\ \mathrm{cm}^{-2}$ for SWCNTs of 0.4 nm [8].

The resistance of CNT via for the both densities $10^{13}\ \mathrm{cm}^{-2}$ and $10^{14}\ \mathrm{cm}^{-2}$ is compared with Cu via for 20 nm diameter connections in Fig. 1 assuming a copper resistivity of $9.5 \times 10^{-8}\ \Omega\,\mathrm{m}$ with 5 nm TiN barrier layer surrounding the Cu wire at this scale. It is clear that for very short structures, a conduction wall density of $10^{14}\ \mathrm{cm}^{-2}$ is required in order to compete with Cu performance. However, for connections longer than 100 nm tubes can out perform copper by one order of magnitude with the conduction wall density of $10^{13}\ \mathrm{cm}^{-2}$ with unprecedented level of thermal conduction and electromigration resistance.

Fig. 2 shows a schematic of different levels of via interconnect in an integrated circuit. In order to integrate CNTs in all levels of interconnection, we need to valid the process technology for different base contact materials. To make a contact on transistor, source, drain and gate, the CNTs should be grown on Si based materials while the metal base contact is used for backend levels. The direct growth of CNT bundles in via holes for VLSI interconnects has been studied by several research groups. Fujitsu is one of pioneers on the integration of CNTs for interconnects and they have presented remarkable works especially focusing on the backend contact using Cu-TiN based back contact materials [9,10]. We consider that the most attractive location in a chip to introduce CNTs interconnects is directly on the source, drain and gate of transistors, and thus to replace the existing first level of connections made with tungsten. Indeed, high aspect ratio vias are required for the first contact level where we can efficiently exploit the advantage of CNTs.

In this work, our trial is to validate the CNT integration in all levels of via interconnects using three different substrate materials, mono crystalline doped Si, poly Si and AlCu compatible to source and drain, gate and backend contacts, respectively.

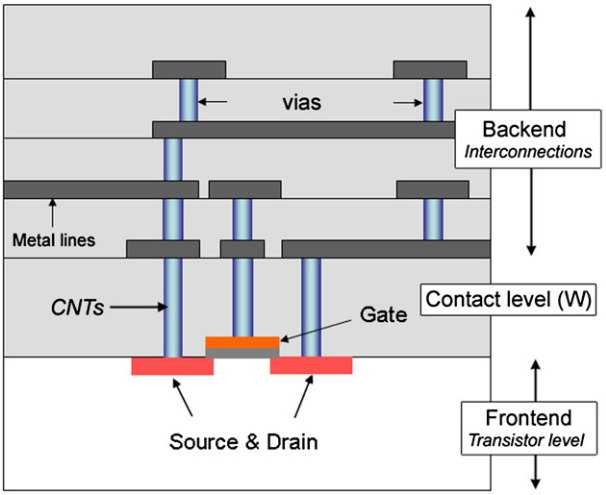

Fig. 2. Schematic cross section of very large scale integrated (VLSI) semiconductor circuit interconnections.

2. Experimental

To develop growth processes on suitable substrate materials to different levels in VLSI circuit interconnections, we choose highly doped mono crystalline Si, poly Si and AlCu (0.4% of Cu in Al) as substrate materials. Experimental conditions are optimized using blanket substrate with representative materials used as base contact in via and then applied to integration in via holes consisting of the same materials as base contacts.

2.1. Dense CNT growth process

Catalysts consisting of a continuous iron film are deposited either by ion beam sputtering (IBS) or electron beam evaporation. The thickness of the Fe film is fixed to be 1 nm for all samples. To obtain a good electrical base contact, all substrates based on Si and Al are deoxidized by dipping in HF solution just before the catalyst deposition. CNTs are grown in a vertical hot-wall Plassys CVD reactor [11]. Differing from conventional classical CVD techniques in a tubular furnace working at the atmospheric pressure, our reactor allows us to perform the growth process at relatively low pressure (∼0.4 mbar). This makes it possible to pre-treat the Fe catalyst in the reactor using an oxidizing plasma. Normally, a step of plasma treatment on the catalyst surface is introduced before the CNT growth at room temperature. RF-plasma power and treatment time are optimized for each substrate. Then the reactor is heated to 600 °C in 15 min under an O_2 or C_2H_2 based atmosphere as a function of the used substrate material. The feed gas mixture is composed with acetylene diluted in H_2 and He. The samples are cooled down under He flow after various growth time (30 min to 1 h for blanket substrate and 5 to 10 min for vias).

2.2. Integration in vias

For test vehicles, materials are chosen attentively for bottom contact in via (metal 1) and top surface in order to enhance and inhibit the CNT growth, respectively. The growth processes are tuned to make no CNT growth on the TiN substrate, which is chosen for the top surface of test vehicles, but an expected growth on the materials of interest for the back contact in vias. This configuration allows us to realize a selective growth only in via holes without catalyst removal on the top of the structure [12]. This simplifies the process for the steps of top contact realization. The bottom material is boron doped silicon (0.014 Ω cm), doped poly Si or AlCu and the insulating material is 600 nm thick silica. A TiN layer of 60 nm is deposited covering the silica. The process flow for vehicle fabrication, catalyst integration and CNT growth is given in Fig. 3. A wet etching step is done to deoxidize the metal 1 just before iron catalyst deposition.

A field emission scanning electron microscope (FE-SEM) LEO 1530 is used to observe the morphology of the grown CNTs both on blanket substrates and in vias. Structure of the grown CNTs are characterized using transmission electron microscope (TEM) Jeol 3010 operating at an accelerating voltage of 300 kV.

3. Results and discussion

3.1. CNT growth on doped Si substrate

In order to optimize the experimental conditions using the Si based substrate, we study the effects of oxidizing plasma pre-treatment of the catalyst. This step is performed at room temperature before the CVD process. It is found that this plasma pre-treatment is the key to master the growth mode and the diameter of grown CNTs. As shown in Fig. 4(a), CNTs with a diameter larger than 8 nm are grown without plasma pre-treatment. The metal catalyst particles are always found at

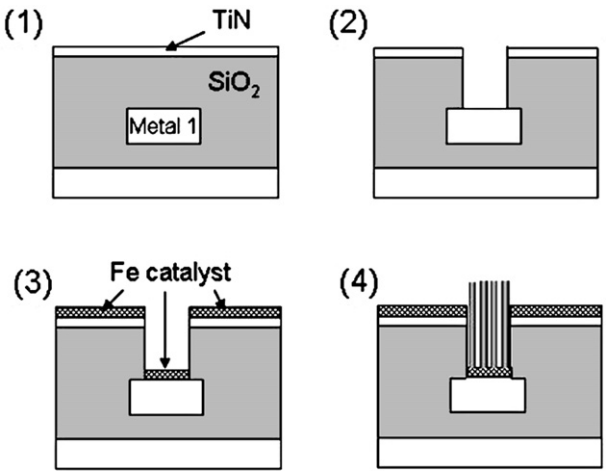

Fig. 3. Process of fabricating via for the integration of CNTs; (1) material stack is deposited, (2) holes are dry etched, and then a wet etch is performed to deoxidize metal 1 (doped Si, poly Si or AlCu), (3) catalyst deposition on whole surface and (4) selective CNT growth in via holes.

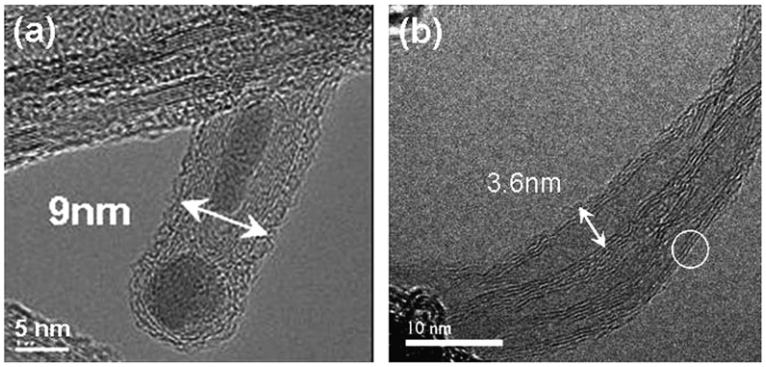

Fig. 4. HR-TEM images of CNTs grown in different growth modes; (a) tip growth mode and (b) base growth mode.

the tip of CNTs, indicating that *tip growth mode* is induced. On the contrary, an addition of plasma pre-treatment step induces *base growth mode*, where the catalyst particles stay at the base of CNT forests. In this case, the observed CNT diameter is much smaller than former case and is less than 5 nm (Fig. 4(b)). In addition, the base grown CNTs lead to higher density than the tip growth ones.

Fig. 5 shows typical morphologies of the base grown CNTs on doped Si substrate by our process with plasma pre-treatment. The grown CNTs are found to form bundles as observed in Fig. 5(b). These bundles consist of 20–30 CNTs (Fig. 5(c)). CNT diameter is observed in the range between 3.5 and 4 nm and the number of wall is 2 or 3 as demonstrated in Fig. 5(d). Particularly the evolutions of CNT density and length as a function of growth time are investigated. An incubation time close to 35 s before CNTs start growing is investigated with our basic process. The film density reaches its maximum for growth time longer than 4 min. The growth time for via test vehicles is thus applied more than 5 min for all experiments.

The process optimized for Si based substrate is tuned to integrate the CNT inside the test vehicles. The integration results are shown in Fig. 6. A very good selectivity for the deposition area is realized after growth. The hole diameters are between 250 nm and 1.5 µm. It can be seen that the yield in holes is 100% and that CNT growth starts from metal 1. Fig. 6(d) demonstrates densified CNTs grown in a via hole. Measuring the diameter of CNT solid after the liquid induced densification [13], we can estimate the density in a focused via hole. The estimated CNT density in a 1.5 µm via hole is around 1.2×10^{12} cm^{-2}. Due to the CNT structure of our films consisting of a mixture of DW and TW, the density of CNT walls in the bundles achieves to 2 to 3×10^{12} cm^{-2}. Considering normal statistical metallic wall content, the expected resistance of the CNT bundle is around 0.7 Ω for 1 µm via with a length of 100 nm; excluding the contact resistance. Electrical confirmation of this value is in progress.

3.2. Process development on poly Si

For the aim if integrating the CNT interconnects at contact level, particularly on *Gate*, our basic process is applied to poly Si substrate. Fig. 7(a) is a result of our first experiment without any tuning of experimental condition to adapt to poly Si substrate. A stable growth is not achieved, where the CNT yield is quite low compared to the case on mono crystalline Si

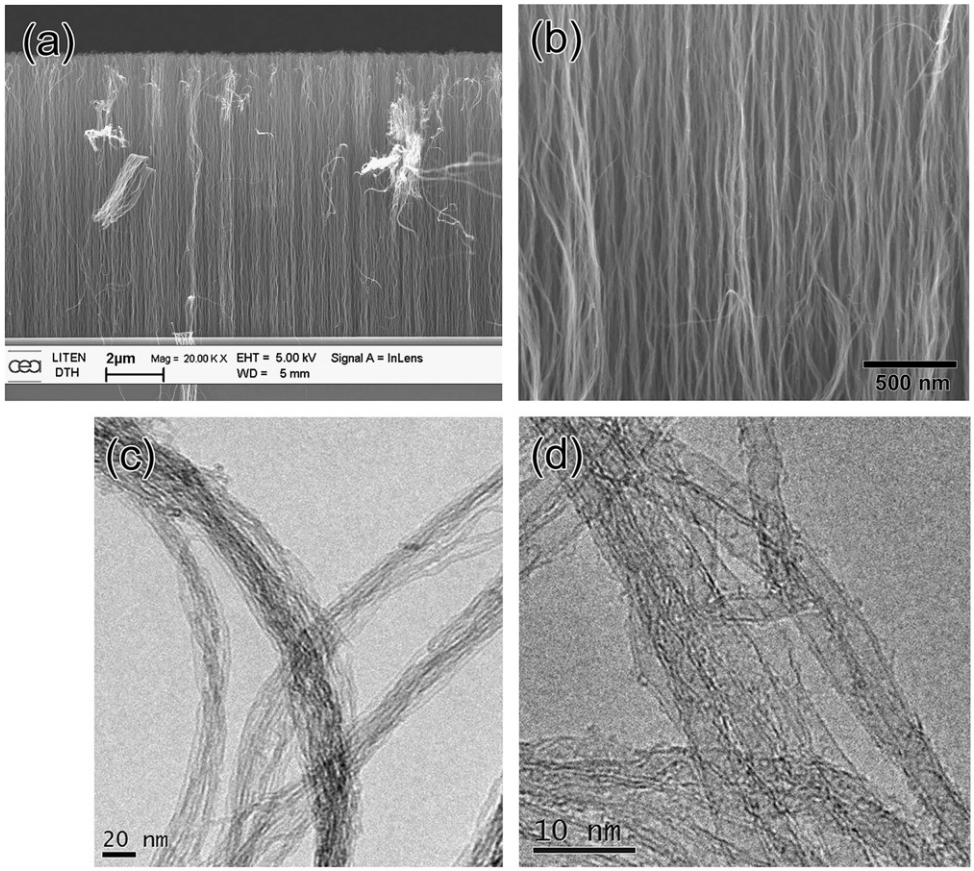

Fig. 5. Typical morphology of vertically aligned CNTs grown on doped Si substrate by our growth process; (a, b) SEM images, (c) TEM image of bundles and (d) typical structure of CNTs.

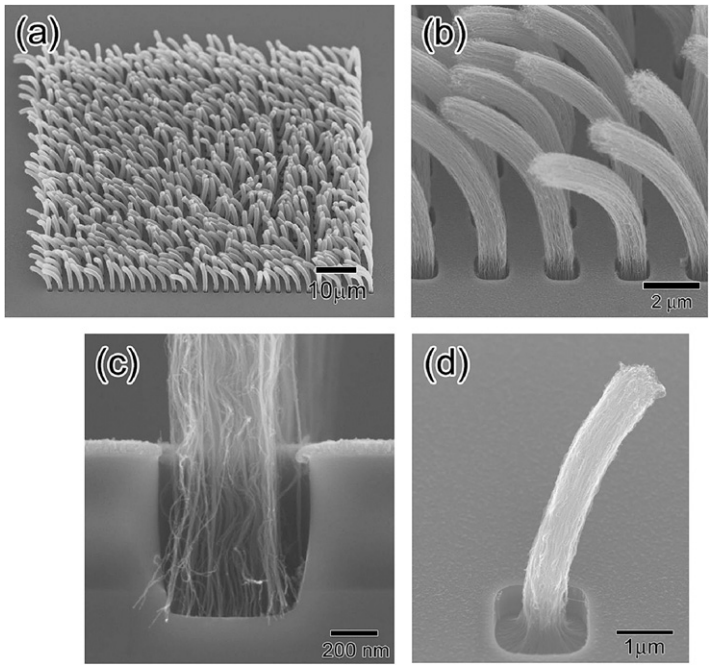

Fig. 6. CNTs grown in via holes with doped Si bottom contact; (a–c) as grown CNTs and (d) CNTs after liquid induced densification.

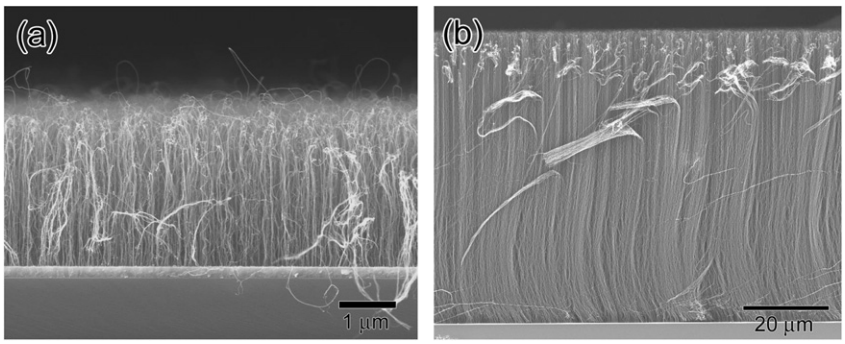

Fig. 7. CNT forests grown on poly Si substrate; (a) under standard experimental condition optimized for doped Si mono crystalline substrate and (b) under conditions with additional oxidizing plasma pre-treatment of Fe catalyst.

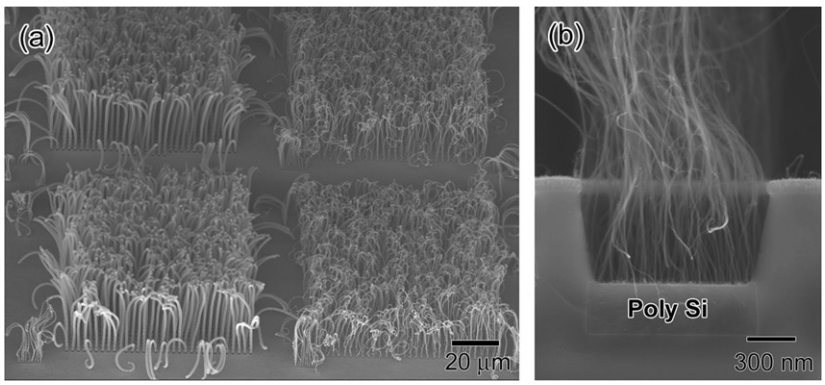

Fig. 8. CNTs grown in via holes with poly Si bottom contacts.

substrate and the CNT density is also lower. In order to adapt the experimental condition to the growth on poly Si substrate, an additional plasma oxidation under higher pressure (2.0 mbar) is inserted before our standard process. Consequently, a base grown high yield CNT forest is obtained, as shown in Fig. 7(b), where the growth rate is more than 60 µm/h.

The base growth mode generally results in a stable growth with high density and small diameter of tubes. As we presented in a previous work [14], the oxidation state of catalyst at the moment of the feed stock gas introduction is an important parameter to define the induced growth mode. Our previous work has demonstrated that to induce the base growth mode the iron catalyst should be oxidized enough before the source gas introduction. Although the iron tends to easily be oxidized even at atmosphere, we need an additional oxidation step because of an exchange of oxygen between the iron catalyst and the Si substrate. Following the Ellingham diagram plotting the free energy of reactions, Fe_3O_4 can be reduced on Si substrate because of the oxidation of Si. Our process optimized for a mono crystalline Si substrate does not induce the same quality of growth on poly Si substrate. The additional oxidation treatment of catalyst is required for the CNT growth on poly Si. It should be due to the presence of a large amount of grain boundary linked with the small grain size (5 to 10 nm) on the substrate surface. Nevertheless, the obtained density is still lower than that on mono crystalline Si substrate. It is supposed to be due to the diffusion of Fe catalyst inside the substrate material through the grain boundary. An increase of Fe catalyst layer thickness to increase the quantity of resulting active catalyst particles could be the solution to obtain the density realized on the mono crystalline Si substrate.

The process with an additional plasma treatment step is thus defined as standard one for the poly Si substrate and applied to test vehicles with poly Si as metal 1. The results of integration are shown in Fig. 8. Almost all via holes are filled with CNTs. However, the tube density is also lower than on the blanket substrate. The growth is very sensitive to the plasma treatment therefore a precise control of plasma performed on whole device surface will be required, especially for application to large scale test vehicles (200 mm).

3.3. CNT growth on AlCu substrate

The integration aimed at the backend metal contact is carried out using an AlCu substrate material. This material has been proposed as an interesting alternative to copper for small dimension lines due to the slower divergence of the aluminum resistivity as compared with copper divergence [15]. Fig. 9(a) shows the CNT grown in via holes. A stable growth is investigated and a 100% filling is also realized. The growth is not sensitive to the plasma pre-treatment and CNTs are grown even without plasma treatment step. Although the used AlCu is poly crystalline, the achieved density is similar or better

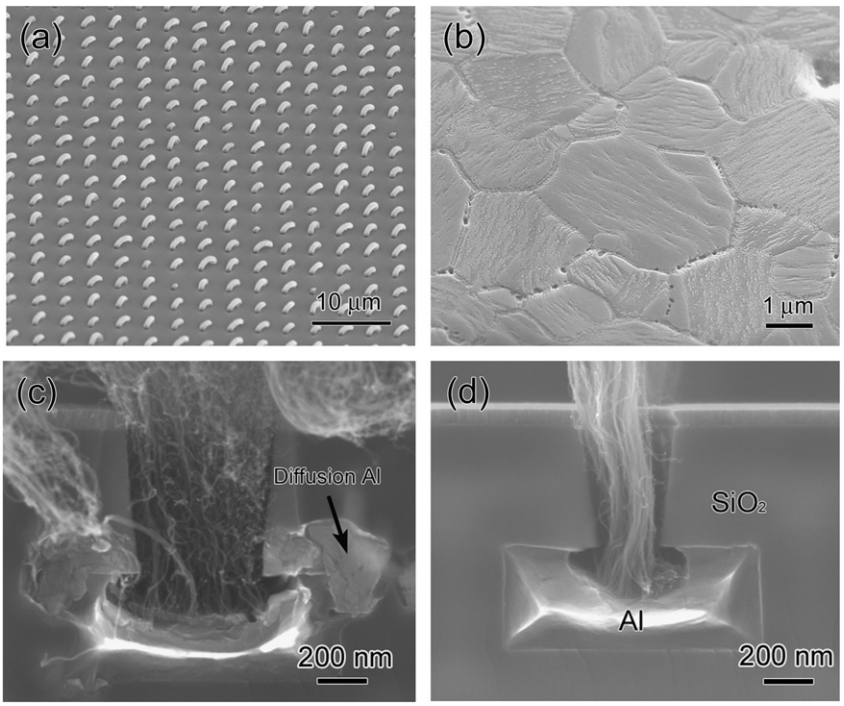

Fig. 9. (a–d) CNTs grown in via holes with AlCu bottom contacts and (c) AlCu diffusion inside SiO_2 dielectric area is investigated after growth at 600 °C and (d) no AlCu diffusion at 580 °C.

to the density achieved on mono crystalline Si. Fig. 9(b) shows a surface of the AlCu substrate used. The grain size is 2 to 3 µm, which is larger than the via hole size, which indicates that no strong influence of the aluminum grain boundary is expected in the growth results.

Fig. 9(c) shows the result of the integration to the test vehicles with AlCu as metal 1 at our standard process temperature, 600 °C. The metal line consisting of AlCu diffused inside SiO_2 dielectric at their contour. In the case of using AlCu as a back contact material, the growth process is influenced neither by the plasma treatment nor by the grain boundary while the device structure is temperature sensitive. We successfully decrease the process temperature down to 580 °C and the result is shown in Fig. 9(d). This temperature is found to be good compromise both for the growth and for the device structure.

4. Conclusions

We have demonstrated the direct integration of CNTs in via interconnections. The experimental conditions were optimized for 3 different back contact materials aiming to the interconnection for different levels of VLSI. We have succeeded to integrate CNTs in via holes with doped Si, poly Si and AlCu as back contacts for source and drain, gate and backend metal lines, respectively. For the use of poly Si, the additional oxidation of a catalyst was needed to struggle against a strong influence of the grain boundary in order to activate the catalyst enough to obtain dense CNT forests. In the case on mono crystalline doped Si we achieved the density of 10^{12} cm^{-2} in a 1 µm via hole with DWNTs and TWNTs, which is expected to give a resistance of 0.7 Ω in 1 µm via. We have demonstrated the capacity for integrating CNTs via interconnects in all levels in VLSI structure using the same process applying some subtle parameter modifications as a function of used back contact materials, which will be quite important requirement for designing the future VLSI circuit with CNTs.

Acknowledgement

This work has been performed in the framework of the European FP7 project Viacarbon funded by the European Commission contract ICT-2007.8.1-216668.

References

[1] A. Naeemi, R. Servari, J.D. Meindl, in: Proceedings of the 44th Annual ACM IEEE Conference on Design Automation, 2007, p. 568.
[2] International Technology Roadmap for Semiconductors (ITRS), 2005 ed., Semiconductor Industry Assoc., 2005.
[3] A. Naeemi, J.D. Mendl, IEEE Electron Device Letters 27 (2006) 338–340.
[4] S. Reich, C. Thomsen, J. Maultzsch, Carbon Nanotubes – Basic Concepts and Physical Properties, Wiley-VCH, 2004.
[5] M.S. Dresselhaus, G. Dresselhaus, Ph. Avouris, Carbon Nanotubes – Synthesis, Structure, Properties, and Applications, Springer, 2001.

[6] F. Kreupl, A.P. Graham, G.S. Duesberg, W. Steinhöegl, M. Liebau, E. Unger, W. Honlein, Microelectronic Engineering 64 (2002) 399.
[7] G.F. Zhong, T. Iwasaki, H. Kawarada, Carbon 44 (2006) 2009–2014.
[8] J.Y. Park, S. Rosenblatt, Y. Yaish, V. Sazonova, H. Ustunel, S. Braig, T.A. Arias, P.W. Bronner, P.L. McEuen, Nano Letters 4 (2004) 517.
[9] A. Kawabata, S. Sato, T. Nozue, T. Hyakushima, M. Norimatsu, M. Mishima, T. Murakami, D. Kondo, K. Asano, M. Ohfuti, H. Kawarada, T. Sakai, M. Nihei, Y. Awano, in: Proc. IEEE Int. Technol. Conf., 2008, pp. 237–239.
[10] M. Katagiri, Y. Yamazaki, N. Sakuma, M. Suzuki, M. Wada, N. Nakamura, N. Matsunaga, S. Sato, M. Nihei, Y. Awano, in: Proc. IEEE Int. Technol. Conf., 2009, pp. 44–46.
[11] T. Goislard De Monsabert, J. Dijon, P. Gadelle, Carbon 43 (2005) 2441–2452.
[12] J. Dijon, A. Fournier, P.D. Szkutnik, H. Okuno, C. Jayet, M. Fayolle, Diamond and Related Materials 19 (2010) 382–388.
[13] D.N. Futaba, K. Hata, T. Yamada, T. Hiraoka, Y. Hayamizu, Y. Kakudate, O. Tanaike, H. Hatori, M. Yumura, S. Iijima, Nature Materials 5 (2006) 987–994.
[14] J. Dijon, P.D. Szkutnik, A. Fournier, T. Goislard de Monsabert, H. Okuno, E. Quesnel, V. Muffato, E. De Vito, N. Bendiab, A. Bogner, N. Bernier, Carbon, in press.
[15] G. Steinlesberger, G. Schindler, M. Engelhardt, W. Steinhogl, M. Traving, in: Proc. IEEE Int. Interconnects Technol. Conf., 2004, pp. 51–53.